Mechanism of Charge Induced Plasma Damage to EPROM Cells During Fabrication of Integrated Circuits

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Abstract Plasma damage mechanisms can be very complex, especially when manufacturing non-volatile memories such as EPROM and flash memories. Plasma damage at via etch can manifest itself as a charge retention failure in the memory cell during product testing. This paper investigates the interaction of UV radiation, classical plasma charging due to non-uniform plasma, and standard integrated circuit fabrication procedures in order to propose an apparent charge loss failure mechanism for non-volatile memories.

Introduction:

Non-volatile memory technology has seen increased use in today's embedded applications. Charge retention is of key concern where non-volatile memories, such as EPROMs, are used to store information in microelectronic circuits.

Plasma induced damage and contamination in RIE processes have been studied extensively in VLSI processes [1-5]. Most plasma-induced damage is done to gate oxides, resulting in transistor threshold voltage shifts. Recently, tunnel oxide degradation in flash memory was attributed to the ultra low leakage current caused by charging damage resulting in stored charge loss [6].

Background:

In a previous paper [7], it was reported that plasma damage was observed at the edges of wafers resulting in charge retention failures of the EPROM memory array during product testing (Figure 1). The activation energy for this charge loss was approximately 0.6 eV. This damage could not be eliminated by using different chamber type, or by varying process pressure, process power or E-chuck voltages. The damage clearly depended upon process chemistry and showed a strong correlation to the presence of ultra violet radiation. It did not resemble the classic gate oxide charging damage reported in literature for logic transistors.

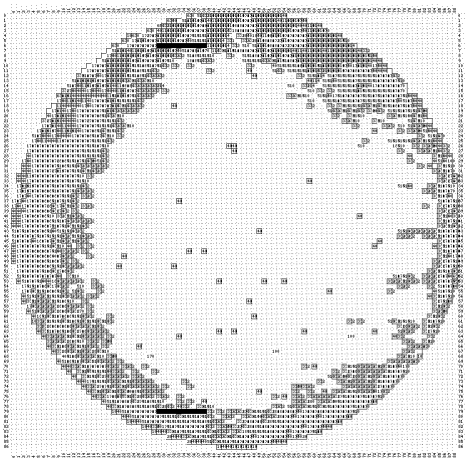

Figure 1
Circuit failure pattern (dark areas)

Non-volatile memories are programmed by storing electrons on a floating gate. These electrons must remain on the floating gate throughout the product life. To screen for potential failure mechanisms, product wafers are subjected to a 250^{o}C bake after programming. If electrons leave the floating

gate, it is considered a charge retention failure. Previously observed damage facts were as follows:

1) Damage was isolated to the plasma via etch step, during which metal and poly antennas become exposed to the plasma.
2) Over-etching at the plasma via etch step did not increase damage.
3) No damage was observed unless vias were open. If the via etch was stopped before via opening, and the etch was completed on a more uniform plasma etcher, no damage was observed.
4) Making the process "center-fast" so that vias opened first in the center did not move the damage to the center of the wafer.
5) The damage was directly proportional to the amount of carbon monoxide in the etch chemistry. Lower CO caused less damage, and no damage was observed in the absence of CO.
6) A direct correlation was observed between UV sensor response on a CHARM-2 [8] wafer and the number of failures.
7) Damage was recoverable. Repeated cycles of programming, 250º C bake and UV erase recovered the devices.
8) Lower pressure and power at the time of opening of vias (i.e. "soft landing") reduced the damage.

Additional Experiments:

Experiments were done to determine if UV alone was causing the damage. CHARM-2 wafers demonstrated both charging and UV signatures. The UV intensity correlated directly with percent carbon monoxide (%CO) and yield as shown in table 1.

The failure pattern on the wafer, shown in figure 1, correlated directly to the CHARM-2 positive potentials shown in Figure 2. The UV distribution was nearly uniform across the entire wafer.

Percent of CO in Etch Process	Average Number of Failing Die	Average UV Sensor Response
0%	0	2.74
5%	8	3.02
22%	18	3.89
36%	50	4.48
85%	169	5.57

Table 1
UV correlation to Carbon Monoxide and failures

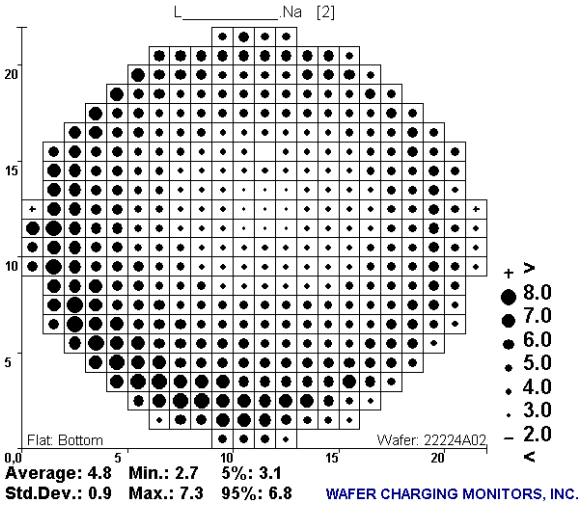

Figure 2
CHARM-2 positive potentials

Upon review of this and other data, it became apparent that the damage was caused by an interaction between UV light and classic wafer charging.

Effect of UV on EPROM Programming:

Earlier work was carried out at Microchip Technology Inc. to investigate how UV erase of EPROM cells works under gate bias conditions [9]. It was shown that with a bias applied to the control gate of an EPROM memory cell during UV erase, the charge stored on the floating gate of the cell could be predicted. This phenomena had the effect of programming the EPROM cell to a threshold voltage that was directly

proportional to the bias voltage applied to the control gate during UV erase (Figure 3).

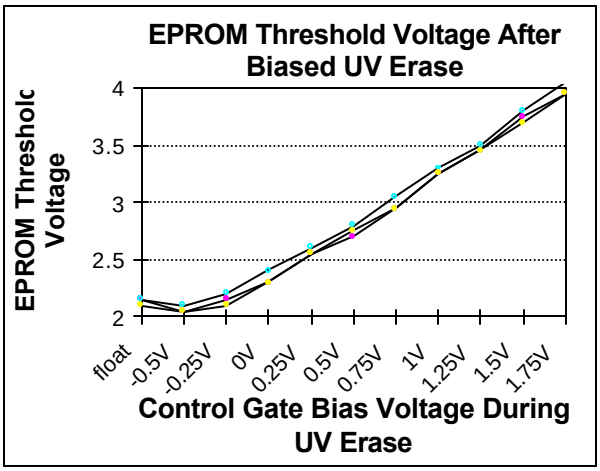

Figure 3
EPROM threshold voltage after biased UV erase

This data suggest that, after via etch, the EPROM memory array may have varying amounts of negative charge stored on the floating gates due to the non-uniform plasma applying a non-uniform bias voltage while UV light is present in the etch chamber. However, having the EPROM cells programmed during processing should not cause damage since this is the intended function of the floating gate memory cell. There must be another piece to the puzzle.

Low temperature post-metallization anneal in forming gas is commonly done in IC fabrication to make Si/SiO_2 interface traps electrically inactive [10]. In our case, the floating gate used to store charge is polysilicon that has many Si/SiO_2 interfaces. It has been shown that forming gas anneal in the presence of negative bias, produces positive traps in the Si/SiO_2 interface with activation energies in the range of 0.3 to 0.6 eV [11,12]. This suggested the possibility that forming gas anneal of EPROM transistors with negatively charged floating gates could be responsible for the charge retention failures.

To confirm this, an experiment was performed using four wafers programmed by an electrical tester. Two of the wafers were then UV erased using a commercial UV lamp. All four wafers were run through the forming gas anneal process. The two wafers that were *not* UV erased prior to anneal exhibited charge retention failure across the entire wafer (Figure 4). The other two wafers exhibited normal test yield with no fallout for charge retention loss.

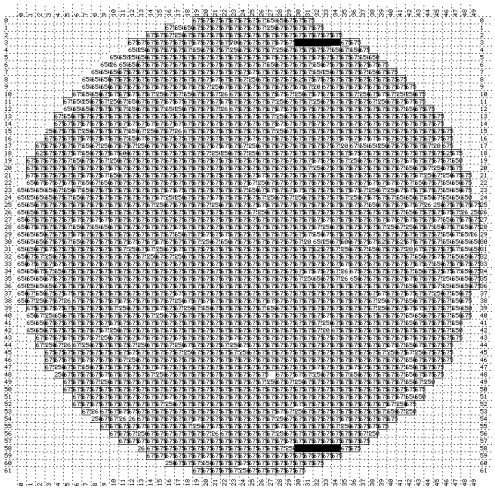

Figure 4
Map of failures from programmed wafer after forming gas anneal. Failures appear dark.

Proposed Mechanism of Damage:

During the via etch, a non-uniform plasma develops a positive potential over the wafer as seen in Figure 2. The presence of CO in different concentrations generates UV light that makes the oxide in the memory array more, or less, conductive. When the metal in the vias is exposed to the non-uniform plasma in the presence of UV light, the memory cells become programmed to different levels according to the radial pattern shown in Figures 1 and 2. This negative charge remains stored on the floating gate during the forming gas anneal step. The hydrogen in the forming gas anneal creates localized high concentrations

of positive-trap sites in the Si/SiO_2 interface area. These positive-trap sites around the floating gate have activation energies low enough to cause electrons to leave the floating gate resulting in margin loss.

This mechanism is consistent with the symptoms of damage shown earlier:

1) Voltage must be present on the control gate of the EPROM cell during UV to cause the problem.
2) Over-etching does not increase damage because the amount of charge stored on the floating gate is a function of bias voltage from the plasma in the presence of UV light.
3) If the vias are not opened, voltage is not present on the EPROM control gate to cause programming.
4) "Center-fast" process did not affect the failure pattern because the pattern was caused by potential distribution due to plasma charging non-uniformity *after* all the vias were opened.
5) UV light is a key factor. As the intensity or wavelength of the UV light is changed, the oxide conductivity is modulated affecting the charge on the floating gate.
6) Same as number 5, above.
7) Repeated cycles of programming, 250ºC bake and UV erase result in device recovery by filling the positive trap sites created by the forming gas anneal.
8) Pressure and other plasma parameters change the voltage non-uniformity. A "soft landing" etch will change how much the EEPROM cells are programmed.

Summary:

This paper demonstrates a mechanism for charge retention failure in EPROM cells due to the complex interaction of UV light and non-uniform plasma potentials during via etch and the forming gas anneal at the end of the process. The UV light and non-uniform plasma potentials cause negative charge to be left on the floating gate after via etch. It is proposed that the hydrogen in the forming gas anneal in combination with negative charge stored on the floating gate causes positive trap sites to be created in the Si/SiO_2 interface resulting in retention failures.

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References:

1. D. Lee, H. Lee, S. Kim and K. Baik, J. Electrochem. Soc., vol. 144 (5) p. 1774, 1997
2. T. Cotler, J. Forster, M. Barnes, and W. Kocon, J. Electrochem. Soc., vol. 141(11) p. 3218, 1994.
3. H. Shin, N. Zha, X. Qian, G. Hills and C. Hu, Solid State Technology, vol. 34(6) p. 29, Aug. 1993.
4. C. Gabriel, J McVittie, Solid State Technology, vol. 34(6) p. 81, June 1992.
5. T. Watanabe, Y. Yoshida, Solid State Technology, vol 26(4) p. 263, Apr. 1984.
6. M. Takebuchi, K. Isobe, T Nashimura, M. Kanda and A. Kimitsuka, 3rd Intl Symposium on Plasma Induced Damage, p. 116, June 1998.
7. C.K. Barlingay, Randy Yach and Wes Lukaszek 6th Intl Symp. Plasma Process Induced Damage, p. 76, May 2001.
8. Wes Lukaszek, Tech. Note 1, Wafer Charging Monitors, Inc., 127 Marine Rd, Woodside, CA 94062.
9. Jack Wong and Randy Yach, Internal Microchip Technology Inc. Publication, 1998.
10. S. Wolf and R.N. Tauber "Silicon Processing for VLSI era," vol 1 Process Technology, (Lattice Press, 1990) p. 222.
11. E. H. Poindexter, J. Non-Cryst. Solids vol. 187, p. 257, 1995.
12. W. L. Warren et al, Appl. Phys. Lett. vol. 68[21], p. 2993, May 1996.