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From the Editor ...

- **Summaries of P²ID papers:** In this issue, we present brief summaries of three CHARM-based papers presented at the 7th International Symposium on Plasma- and Process-Induced Damage (June 2002).

Where appropriate, we quote directly from the original papers. You may obtain copies of the complete papers from WCM.

- **We now distribute this bulletin only by e-mail.** Please alert your colleagues to send their e-mail addresses and company name to bulletin@charm-2.com to get a free subscription to the Wafer Charging Bulletin. (There will be no sales call.)

Wanted: Source of 300 mm wafers

We are trying to locate a manufacturer for 300mm CHARM-2 wafers. The CHARM-2 wafers are built on an EEPROM technology. If you know of a potential candidate, please contact us.

New and exciting ...

Automated ChargeMap™ ready for release!

We are pleased to announce the release of a new version of ChargeMap – the CHARM-2 data analysis and interpretation software.

The new version of ChargeMap generates the appropriate wafer maps, J-V plots, and a complete report of all findings automatically – a click on the “Analyze” button does it! The new report format now includes extensive explanations of the results, and their relevance to charging damage.

ChargeMap also verifies the integrity of the calibration, program, and measure data files to ensure a fool-proof assessment of the charging characteristics of your process tools.

The new ChargeMap also includes DamageMap™, which summarizes in a single wafer map the results displayed in several J-V graphs. Given the gate oxide breakdown voltage, DamageMap produces a wafer map of charging currents, the real cause of charging damage. DamageMap

wafer maps may be compared directly to product yield wafer maps, to determine if a particular processing tool is responsible for damage to product gate oxide.

Summaries of P²ID papers ...

Utility of CHARM^â-2 in Diagnosing Sources of Plasma Charging Damage in High Density Etchers and in Assisting Hardware Development

(S. Siu, R. Patrick, and V. Vahedi, Lam Research Corporation)

In this paper, the authors discussed several case studies (there were more) which illustrated the range of charging problems resolved at Lam Research Corporation through the use of CHARM-2 charging monitors.

The authors used CHARM-2 wafers to address customer yield problems, hardware issues with existing equipment, and hardware development problems. In all cases, the problem-solving procedure involved characterizing the initial state of equipment using CHARM-2 wafers, followed by process or equipment adjustments designed to minimize or eliminate the CHARM-2 signals. When this was accomplished, the problem was eliminated. The case studies were as follows:

a) NON-UNIFORM PLASMA: In case of the non-uniform plasma, whose signature is shown in Figure 1, “it was ...determined that the top to bottom power ratio was too low – this resulted in the plasma being driven by the bottom RF which led to a very non-uniform center to edge plasma. Splits run on CHARM-2 showed that increasing top power by 2X reduced the charging signature ..., and reducing the bias by ½ eliminated all charging... When this returned process was tested on the customer product lot, the profiles met specifications, and the yield problem was eliminated.”

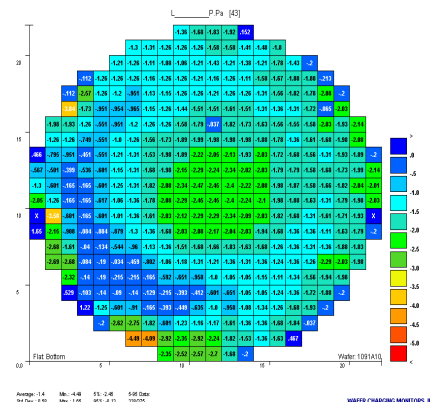


Figure 1. Negative potentials caused by plasma non-uniformity due to improper top to bottom power ratio.

b) IMPROPERLY ADJUSTED LIFTER PINS: Wafer pins touching the backside of the wafer caused yield loss in the center of the wafer which mirrored the CHARM-2 charging pattern shown in Figure 2. “Once the customer had the lifter pins properly adjusted, the charging pattern disappeared and the yield levels returned to normal.”

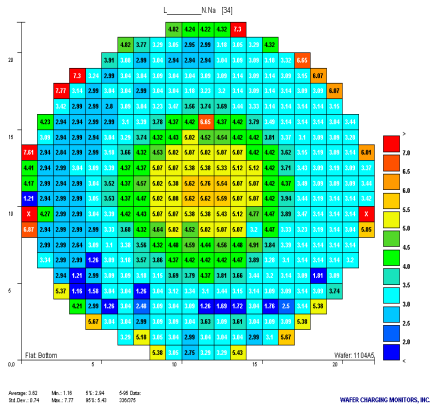


Figure 2. Charging pattern causing yield loss due to lifter pins touching the backside of the wafer.

c) MONOPOLAR ESC: When “CHARM-2 was used to diagnose a charging problem stemming from *monopolar* electrostatic clamping... it was discovered that the sequencing of the plasma ignite and ESC ON steps were crucial to avoiding charging damage. It was found that if the ESC was turned ON before the plasma was ignited, a large positive CHARM-2 signature was seen (sensors saturated). In the case where the plasma is ignited first, the wafer potential is held near the plasma potential, and the subsequent ESC chucking voltage will not induce charging damage. Subsequent CHARM-2 tests with this sequence showed no charging, and subsequent steps have been taken to ensure that etchers with monopolar chucks have the proper turn on sequence.”

d) NON-UNIFORM RF IN HIGH-TEMPERATURE ESC: When “a high temperature ESC was being prototyped, as part of the standard procedure in the development work, the ESC was tested with a CHARM-2 wafer. An unexpected large CHARM-2 signature was seen. Later work showed that there was a large variation in the ESC dielectric, and this variation correlated to the charging map generated by CHARM-2, as shown in Figure 3 ... Needless to say, this ESC was promptly decommissioned.”

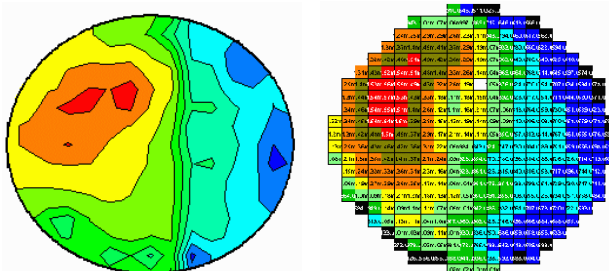


Figure 3. Comparison of ESC dielectric thickness (left) and charging current distribution on CHARM-2 wafer (right).

e) NON-UNIFORM RF DUE TO PARTICLE ON ESC: Another type of “non-uniform RF coupling through the wafer was seen ... where there was a large Si particle (100-200 μm diameter) on the ESC. ... The wafer did not chuck

properly, and the non-uniform gap between the wafer and the ESC top surface generated a non-uniform RF drop across the wafer resulting in a large positive and negative gradient across the wafer, as shown in Figure 4. ... Once the ESC was cleaned, the charging was eliminated.”

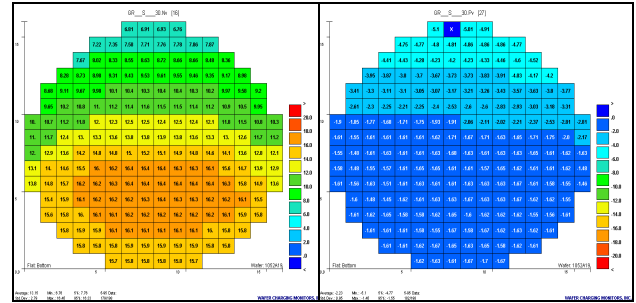


Figure 4. Positive and negative charging gradients caused by a 100-200 μm particle (at top) on the surface of an ESC.

f) BAFFLE FOR DOWN STREAM ETCHER: The “last case shows the utility of CHARM UV sensors in assisting hardware design. In prototyping work on baffle design for a down stream etcher, it was important to block the ions and UV from the wafer. ... CHARM-2 was used to ensure that baffle design did indeed block all ions and UV at the wafer level. Although the non-optimized baffle did not permit ions to reach the wafer (CHARM-2 map was clean), the baffle did allow UV through, as shown in Figure 5. With the final optimized baffle design, all the reflections were eliminated, and there was no UV response from CHARM-2.”

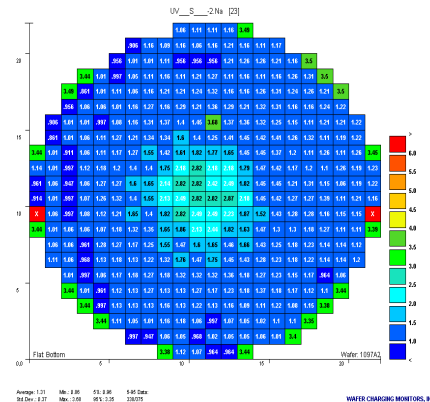


Figure 5. Non-optimized baffle causes UV to reach the center of the wafer in a down stream etcher.

Mechanism of Charge Induced Plasma Damage to EPROM Cells During Fabrication of Integrated Circuits

(C.K. Barlingay and R. Yach, Microchip Technology, and W. Lukaszek, WCM)

This paper illustrated how the interaction of UV and positive potentials in a non-uniform plasma oxide etcher (via etch), in combination with negative-bias-temperature-instability (NBTI), resulted in a very difficult yield problem on EPROM products. (This problem could affect EEPROM and flash products, as well.)

The problem manifested itself as charge-loss on programmed EPROM transistors after a 24 hour, 250 °C bake. Surprisingly, repeated UV erase and bake cycles reduced the amount of subsequent charge loss – the EPROM transistors appeared to improve! (Typically, charge-loss problems get worse with repeated program-erase cycling.)

When the threshold voltages of process monitor logic transistors were mapped over the wafer, no threshold shifts were observed, indicating no damage to logic transistors. However, the as-manufactured EPROM transistors showed increasing thresholds toward the edge of the wafer, which correlated with the charge loss-related yield loss, shown in Figure 6(a).

The yield loss, in turn, correlated nicely to CHARM-2 positive potentials, shown in Figure 6(b). Surprisingly, however, over-etching the vias did not increase yield loss, indicating that it was not caused by positive charging from electron shading. This, in turn, led to a conjecture that UV might also be involved.

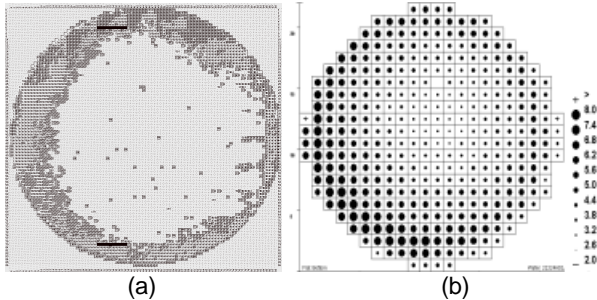


Figure 6. (a) Die failing charge loss (in black); (b) CHARM-2 positive potentials.

Supporting evidence for this conjecture came from additional experiments which revealed that the number of failed die varied with the amount of CO in the etch gas mixture, as shown below. The number of failed die, in turn, correlated well with the CHARM-2 UV sensor response.

Percent of CO in Etch Process	Average Number of Failing Die	Average UV Sensor Response
0%	0	2.74
5%	8	3.02
22%	18	3.89
36%	50	4.48
85%	169	5.57

These observations led to a hypothesis that the combination of UV and high positive potentials, during the via etch step, programmed the EPROM transistors to high threshold voltages, and this somehow led to EPROM charge loss. Indeed, previous experience with EPROM UV erase showed that when EPROM control gates are biased and simultaneously exposed to UV, EPROM transistors can be programmed to different threshold voltages using gate biases much lower than normally necessary for EPROM programming, as shown in Figure 7.

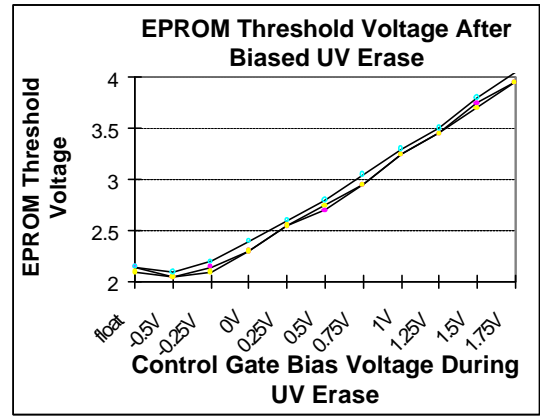


Figure 7. EPROM programming during UV exposure.

As confirmation that EPROM transistors programmed to sufficiently high threshold voltages were responsible for the yield loss, all die on several product wafers were programmed on a functional tester and sent through a forming gas anneal. The charge loss-related yield loss (nearly 100%) is shown in Figure 8.

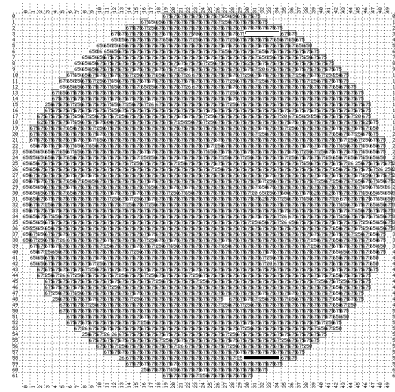


Figure 8. Die failing charge-loss (in black; nearly 100%) on a tester-programmed wafer.

So why did programmed EEPROM transistors experience subsequent charge loss? The proposed answer involves negative-bias-temperature-instability (NBTI) – an old (but re-emerging) mechanism where, under negative gate bias, hydrogen interacts with silicon dioxide to form positively charged traps near a negatively-biased gate. (Since a programmed EEPROM transistor contains electrons on the floating gate, it satisfies this condition during the forming gas anneal.) Consequently, the positively-charged traps near the floating gate absorbed some electrons from the floating gate, leading to charge loss during a 24 hour, 250 °C bake. Since not all traps were filled during the first bake, subsequent UV erase/program/bake cycles caused additional filling of traps. However, the number of traps is finite so their number decreased with each erase/program/bake cycle, leading to smaller charge loss from the floating gate with each erase/program/bake cycle, i. e., the EPROM transistor appeared to improve!

Although observed on EPROM transistors, it is probable that similar behavior would occur on EEPROM or flash devices in similar circumstances.

Impact of F Species on Plasma Charge Damage in a RF asher

(S. Q. Gu, R. Fujimoto and P. McGrath, LSI Logic)

As the incorporation of fluorine in ashing chemistries was known to facilitate removal of ion implant-hardened resist and side wall polymers formed during via etching, the authors explored “the usage of a combination of RF and MW for photo resist ashing and cleaning, and the effect of the RIE components of plasma on plasma charging” in the presence of C_xF_y and NF_3 chemistries.

To evaluate plasma charging, the authors used “device wafers with gate oxide thickness ranging from 60 to 110 Å”. In comparison to the old solvent clean process, the new plasma process caused charge damage to devices in the center of the wafer.

To quantify plasma charging under different plasma conditions, the authors used CHARM-2 wafers. It was observed that an RF-only plasma and $O_2/N_2:H_2 / C_xF_y$ chemistry did not cause any charging, but an RF/MW plasma using the same gas chemistry caused charging in the center of wafer, as shown in Figure 9(a). However, when $O_2/N_2:H_2/NF_3$ chemistry was used with RF-only plasma, positive charging was again observed in the center of the wafer, as shown in Figure 9(b).

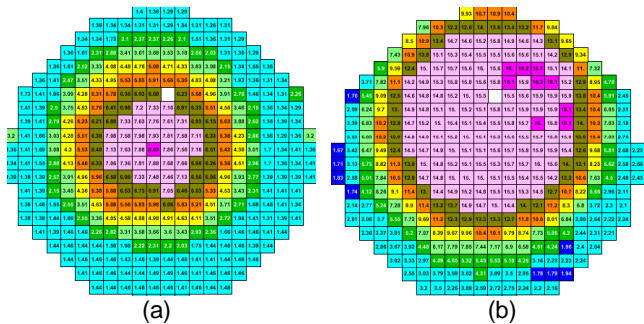


Figure 9. (a) Positive charging from RF/MW plasma using $O_2/N_2:H_2 / C_xF_y$ chemistry; (b) Positive charging from RF-only plasma using $O_2/N_2:H_2/NF_3$ chemistry.

To understand the underlying cause of charging, the above plasmas were also analyzed using optical spectroscopy. The net contribution of F based chemistries to the plasma is shown in Figure 10.

The authors explain the RF vs. MW power dependence of free fluorine density as follows: “When C_xF_y passes the MW applicator, MW power will break C_xF_y into F and other C_mF_{y-n} . The RF power is less effective in breaking C_xF_y bonds to form free F. NF_3 on the other hand is much more easier gas to dissociate in a plasma.”

The authors conclude that “CHARM-2 wafers show high plasma charge voltage for all three plasma that exhibited free fluorine emission. In addition, no plasma charge voltage was observed on the $O_2/N_2:H_2 / C_xF_y$ RF plasma using the CHARM-2 approach which is consistent with no free Fluorine emission as observed by optical spectroscopy. This suggests that the plasma charge is sensitive to the combination of RF and density of free F species.”

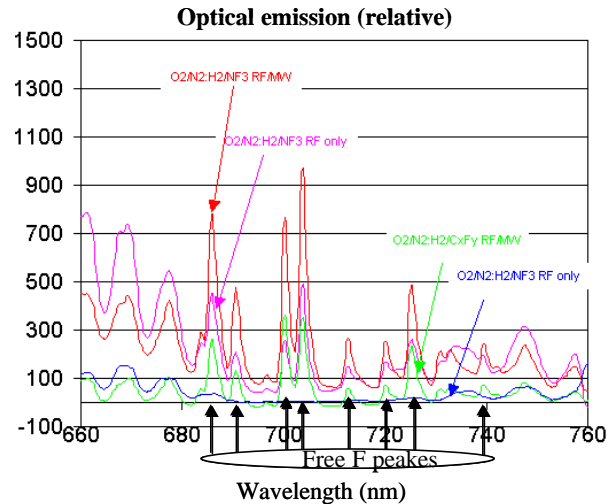


Figure 10. The net emission spectrum of: C_xF_y addition for RF-only plasma; C_xF_y addition for RF/MW plasma; NF_3 addition only; and NF_3 addition for RF/MW plasma after subtracting the base $O_2/N_2:H_2$ spectra.

ACKNOWLEDGMENTS:

We are very grateful to our colleagues at Lam Research, LSI Logic, and Microchip Technology for their permission to use excerpts from their papers in this Bulletin.

FUTURE TOPICS:

In the next issue, we will review our P^2ID paper, which compares electron shading effects in uniform and non-uniform plasma oxide etchers. We will also present a summary of our upcoming IIT’2002 paper which examines patterned-resist charging in high-current ion implanters. This will give us the opportunity to compare in the same issue charging effects in high-density plasmas vs. charging effects in high-current ion implanters when using the same feature sizes. You’re in for a surprise!

HOW TO CONTACT WCM:

If you would like to receive this bulletin or information about our products, services, and publications, or would like to contribute material to this bulletin, please contact:

Wafer Charging Monitors, Inc.
 127 Marine Road, Woodside, CA 94062
 phone: 650-851-9313 / fax: 650-851-2252
 web site: www.charm-2.com
 email: sales@charm-2.com

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