

## WAFER CHARGING DAMAGE IN IC PROCESS EQUIPMENT

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Wafer charging damage in IC process equipment is the result of complex interactions between the wafer environment and the wafer. Quantifying the UV and charging characteristics of process tools, understanding the interactions between the wafer environment and the wafer, and recognizing the relative importance of the different mechanisms capable of causing damage are all important for successful diagnosis and control of charging damage during wafer manufacturing. This paper discusses these topics, and illustrates them with examples from experiments conducted in different process tools.

### INTRODUCTION

Product charging damage in IC processing equipment has been a recurring problem in IC manufacturing for nearly two decades. Although significant effort is devoted by equipment makers and IC manufacturers to control wafer charging, new charging mechanisms emerge as equipment designs change and IC technologies are scaled for higher performance. Because charging damage in IC process equipment is the result of complex interactions between the wafer environment and the wafer, understanding charging damage is an on-going challenge. This paper reviews the current state of understanding, illustrates it with examples from experiments conducted on different process tools, and briefly discusses the interactions between charging sources and device structures which determine the extent of device damage.

### BASICS OF CHARGING DAMAGE

Although understanding damage to insulators during wafer processing can be complicated by many details, the underlying concepts are relatively simple. Typically, damage to thin insulators (gate oxides) sandwiched between a conductive substrate and isolated conductive electrodes on the surface of a wafer (gates) occurs due to *current flow* through the insulator, driven by a potential difference between the surface electrode and the substrate (1). Even when the substrate is electrically floating, differences in potential between electrodes located in different portions of a wafer can cause current flow from one set of electrodes to the other through the insulators and the substrate.

During wafer processing, global (wafer scale) potential differences are caused by global non-uniformities in plasma density and/or electron temperature (2) or, in the case of ion-beam equipment, by spatially imperfect neutralization of the charging caused by

the ion beam. Both of these mechanisms cause imbalances between ion and electron fluxes that give rise to different electrode-substrate potentials over large areas of the wafer. (*Highly localized* charging events scattered over a large area are also sometimes observed in plasma equipment.) Charging damage in processes where the electrodes are entirely exposed, such as resist stripping (3) is typically associated with global variations in surface charging. Likewise, charging damage during oxide depositions is associated with global variations in surface charging (4), or a combination of surface charging and UV (5).

Moreover, even in uniform plasmas, highly localized charging due to *local* imbalance in ion and electron fluxes associated with holes-in-insulator topographical features may cause gate oxide damage. This localized charging, called “electron shading” (6) is due to negative charging of the insulator (e. g. resist) which prevents low energy electrons from reaching the bottom of the hole to neutralize the positive ion flux, thereby causing net positive charging at the bottom of the hole. The magnitude of this fundamental effect increases with increasing aspect (height/width) ratio. Charging damage in etching processes is caused by a combination of global and localized charging. The localized charging caused by “electron shading” is superimposed on the global charging effects.

Another variable which influences the magnitude of the potentials and currents experienced by device structures is the area of charge collecting electrodes (antennas) connected to the substrate (7,8). This effect is not surprising, since any connections to the substrate will influence the substrate potential, which, in turn, affects the surface-substrate potential difference experienced by gate oxide.

## DISCUSSION OF EXPERIMENTAL RESULTS

### Charging Monitor

Before illustrating these mechanisms with experimental results, a brief look at the tool used to collect the data presented in this paper. The data was obtained with the CHARM<sup>®</sup>-2 monitors<sup>1</sup>, which are implemented as monolithic silicon wafers populated with microscopic, EEPROM-based potential, charge-flux, and UV sensors (9).

The potential sensors are implemented by connecting a charge collection electrode (CCE) on the surface of the wafer to the control-gate of an EEPROM transistor, as shown in Figure 1a. The potential sensors are calibrated to measure the surface-substrate potential in volts. Separate sensors are used to measure positive potentials and negative potentials.

The charge-flux sensors are implemented by adding current-sensing resistors between the CCE and the substrate of the potential sensors, as shown Figure 1b. In this configuration, EEPROM transistors measure the voltage across the current-sensing resistors, from which current density is calculated. The charge-flux sensors are calibrated to measure the net charge-flux in A/cm<sup>2</sup>. Separate sensors are used to measure positive charge flux and negative charge flux. Since one sensor provides a single point in

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<sup>1</sup> CHARM<sup>®</sup>-2 monitors are available from Wafer Charging Monitors, Inc., Woodside, CA. CHARM<sup>®</sup> is a registered trademark of Wafer Charging Monitors, Inc.

the J-V plane, data from many sensors is used to construct the positive or negative J-V characteristics of the charging source<sup>2</sup>.

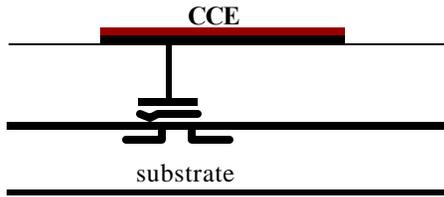


Figure 1a. CHARM<sup>®</sup>-2 potential sensor.

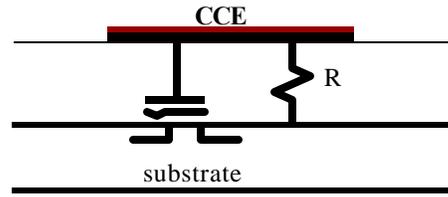


Figure 1b. CHARM<sup>®</sup>-2 charge-flux sensor.

### Charging in Ion Implantation

Let's now begin our examples of charging phenomena with a brief discussion of charging in ion implantation. When devices are under the beam in a high-current ion implanter, they are exposed to positive charging from the high-energy ion beam, from "slow" ions (ionized background gases or the plasma used for charge neutralization), and from secondary electrons emitted from the surface of the wafer due to ionic impact. They are also exposed to negative charging from the "electron shower" or the plasma electrons from the plasma flood system used to neutralize positive charging. Therefore, the *net* positive charging when devices are under the beam is the sum of the positive and negative charging just described. On the other hand, when devices are outside the beam, they experience only negative charging from the "electron shower", or from the plasma flood system, used to neutralize positive charging (10).

The balance between positive and negative charging, controlled by the "electron shower" or a plasma flood system, is illustrated in Figures 2a and 2b.

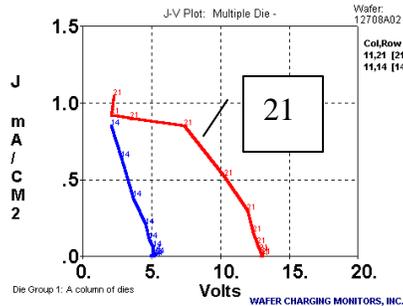


Figure 2a. Positive J-V plots recorded at two different locations on a wafer during a high current ion implant.

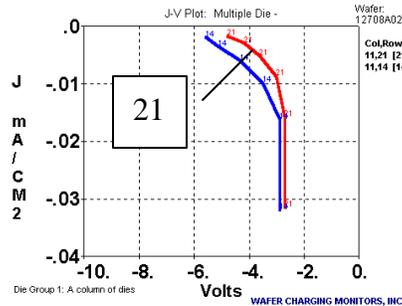


Figure 2b. Negative J-V plots recorded on the same wafer during a high current ion implant.

Higher positive charging in die (11,21), curve 21, shown in Figure 2a, is associated with lower negative charging, shown in Figure 2b. Conversely lower positive charging in die (11,14), curve 14, is associated with higher negative charging. In this case, the spatially non-uniform output of the charge neutralization system gave rise to spatially non-uniform positive charging.

<sup>2</sup> For a discussion of J-V plots and their application to prediction of charging damage, refer to WCM Wafer Charging Bulletin, Vol. 1, No. 1, available from WCM website: [www.charm-2.com](http://www.charm-2.com)

**Charging in High Density Plasmas**

A typical spatial relationship between positive charging, negative charging, and UV intensity in a “simple”, high-density plasma is shown in Figures 3a-3c. In this case, the positive potentials are highest around the perimeter of the wafer, whereas negative potentials are highest in the center of the wafer. The high positive potentials around the perimeter of the wafer indicate a region of higher plasma density, which is consistent with lower UV emissions<sup>3</sup>, as shown in Figure 3c. The high plasma density causes positive current to enter the wafer around the perimeter, as shown in Figure 3d, and leave through the center of the wafer<sup>4</sup>, as shown in Figure 3e. (The complementary relationship between the potential wafer maps and UV wafer map makes it easy to confuse the response from UV with the response from charging when using the contactless techniques which employ oxidized wafers as charging monitors.)

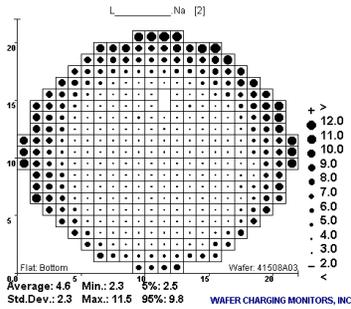


Figure 3a. Positive potentials in a HDP.

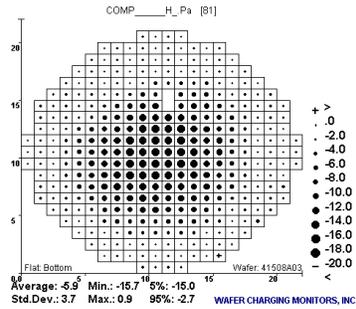


Figure 3b. Negative potentials in a HDP.

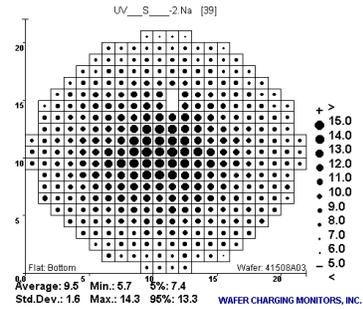


Figure 3c. UV intensity in a HDP.

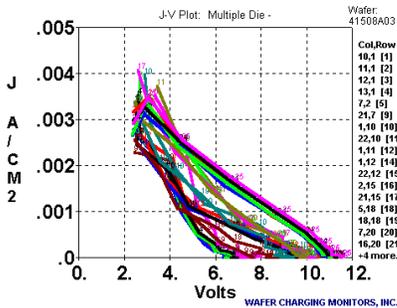


Figure 3d. Positive current enters the wafer around wafer perimeter.

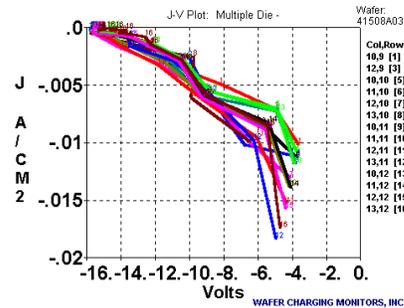


Figure 3e. Negative current is observed in the center of the wafer current leaves through the center of the wafer.

The complementary behavior illustrated in Figures 3a-3e can take on many different forms. For example, gradient patterns are often observed when positive charging occurs on one side of the wafer and negative charging occurs on the opposite side of the wafer.

Occasionally, instabilities occur which cause highly localized charging scattered over a significant portion of the wafer, as illustrated in Figures 4a – 4c. Figure 4a shows what appears to be random negative charging. However, when the maximum value from four identical sensors is displayed, it becomes clear that charging was not random, and that the most intense activity occurred in the center of the wafer, as shown in Figure 4b. The

<sup>3</sup> In HDP, higher plasma density leads to lower UV emissions, whereas the opposite is true for LDP.

<sup>4</sup> Current is defined here as the flow of positive charge (EE sign convention).

irregular (“zig-zag”) nature of the negative J-V plots (obtained by combining data from many sensors in each die), shown in Figure 4c, confirms that different sensors within the die experienced very different charging conditions. Because the sensors are only millimeters apart, we conclude that very intense, highly localized charging events occurred in the center of the wafer.

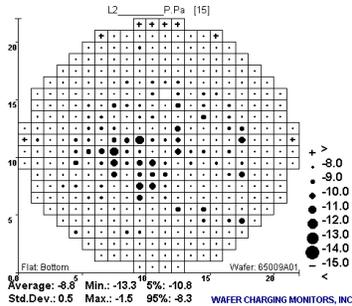


Figure 4a. Negative potentials recorded by a single sensor in a die.

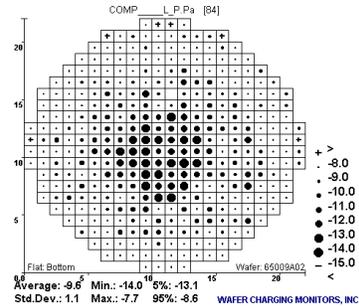


Figure 4b. Highest negative potentials recorded by one of four sensors in a die.

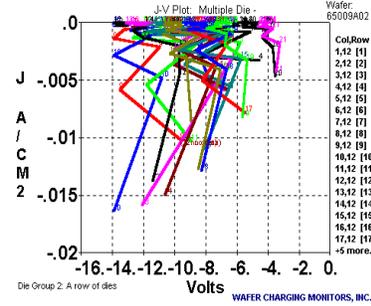


Figure 4c. Negative J-V recorded in the central portion of the wafer.

Pattern-Induced Charging Effects (“Electron-Shading” in Uniform Plasma)

The localized charging effect (“electron shading”) caused by hole-in-insulator topographies is illustrated in Figures 5a, 5b, and 5c. Figure 5a is a wafer map of positive potentials obtained in a plasma oxide etcher using a bare wafer (no topography). The potentials are low and uniform over the entire wafer, indicating good plasma uniformity.

On the other hand, Figure 5b is a wafer map of positive potentials obtained in the same oxide etcher using a wafer covered with photoresist patterned with holes using electron-beam lithography. Significantly elevated potentials in the different sites illustrate the effect of the twelve different designs which used different size and number of holes in the resist over the charge-collection-electrodes.

Figure 5c illustrates the aspect-ratio dependence of the localized, topography-induced charging. Both peak potentials and current densities measured with the 0.3um hole pattern are higher than those obtained for the 0.6um hole pattern (11).

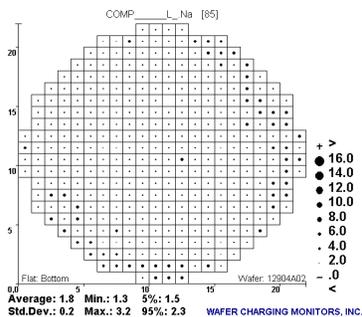


Figure 5a. Positive potentials in an oxide etcher recorded with a bare wafer.

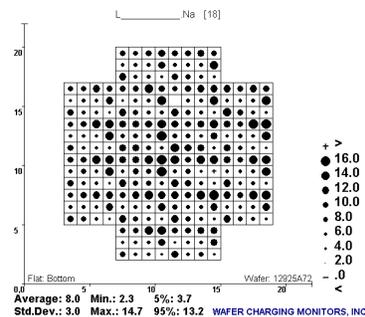


Figure 5b. Positive potentials in an oxide etcher recorded with a wafer covered with patterned resist.

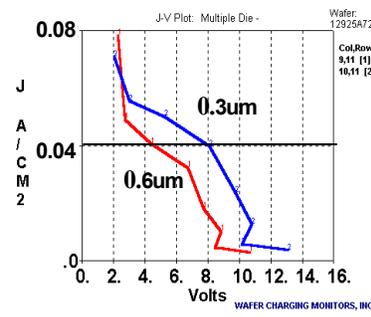


Figure 5c. Positive J-V in 0.6 um and 0.3 um resist holes measured in an oxide etcher.

“Electron-Shading” in Non-Uniform Plasma

When patterned resist wafers are processed in a tool which exhibits plasma non-uniformity, the “electron shading” and plasma non-uniformity effects add, as shown in Figures 6a –6d. Figures 6a and 6b show the positive potentials on a bare and resist-patterned wafer in an oxide etcher. The non-uniformity of the distribution is preserved on the resist-patterned wafer, but the potentials recorded in the 1.5 um holes are considerably higher than on the bare wafer due to the “electron-shading” effect. The same trend is evident in the positive J-V plots. Figures 6c and 6d show the positive J-V plots obtained in the same three die. On the bare wafer, the edge-most die shows a response, the other two die in the plot do not. (The vertical asymptote at ~ 2.6 V indicates non-responding sensors.) The corresponding positive J-V plots obtained on the resist covered wafer are shown in Figure 6d, where J-V plots are recorded in all three die.

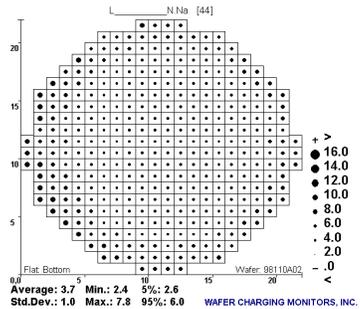


Figure 6a. Positive potentials on a bare wafer in an oxide etcher.

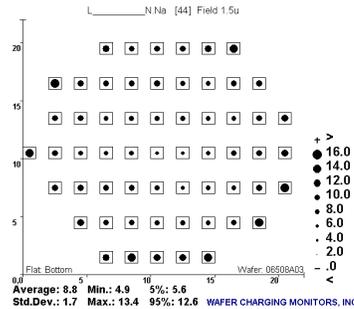


Figure 6b. Positive potentials recorded in 1.5 um resist holes in an oxide etcher.

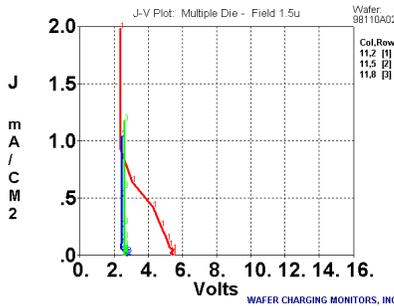


Figure 6c. Positive J-V on a bare wafer in an oxide etcher.

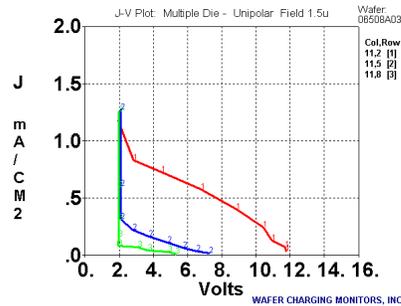


Figure 6d. Positive J-V recorded in 1.5 um resist holes in an oxide etcher.

“Anomalous” Charging Phenomena

The previous examples support the widely accepted plasma non-uniformity and the “electron shading” charging models. However, additional effects exist for which adequate models have not been established. Figures 7a-7d compare positive potentials and J-V plots obtained in an oxide etcher with a bare wafer and a wafer covered with photoresist patterned with a product via mask (9). The plasma non-uniformity, evident in the positive potentials and J-V plots obtained with a bare wafer, and shown in Figures 7a and 7b, is significantly amplified by the presence of the patterned photoresist, as shown in Figures 7c and 7d.

In particular, the positive J-V plots shown in Figure 7d were obtained from uncovered sensor locations coinciding with the product mask 100um-wide scribe lanes. (The J-V plots are irregular due to mis-alignment of open areas in the product mask and the

CHARM<sup>®</sup>-2 wafer layout.) The dramatic increase in positive potentials and current densities in these locations cannot be attributed to the topography-dependent “electron shading” effect (the aspect ratio is very low). A quantitative model for this phenomenon does not exist.

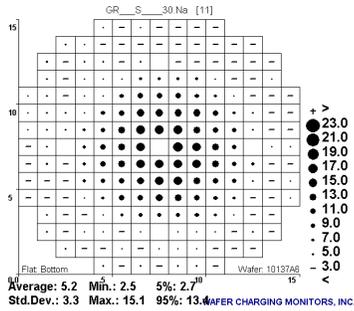


Figure 7a. Positive potentials on bare wafer.

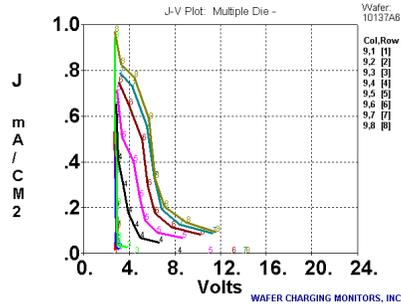


Figure 7b. Positive J-V plots obtained on bare wafer.

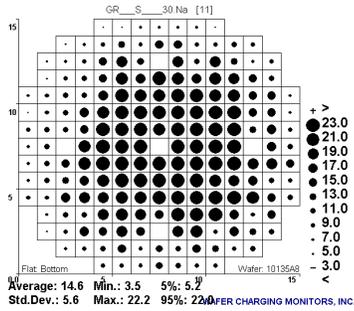


Figure 7c. Elevated positive potentials on wafer covered with resist, patterned with product via mask.

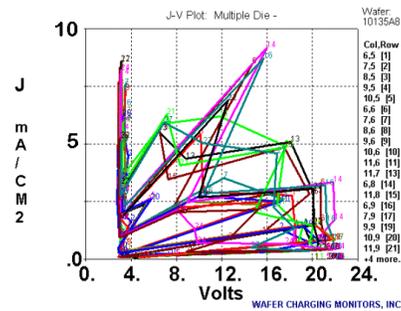
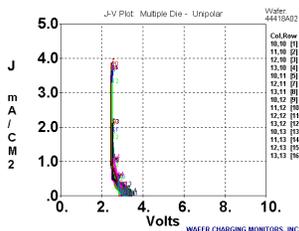
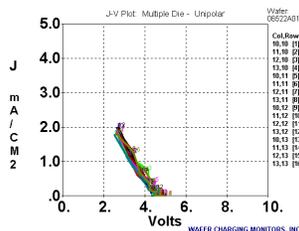


Figure 7d. Positive J-V plots obtained on wafer covered with resist, patterned with product mask.

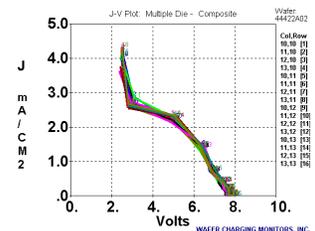
Another effect which can modulate wafer potentials and J-V plots in process tools occurs due to substrate connections. When the area of charge-collecting electrodes connected to the substrate decreases, the wafer potentials increase (and J-V plots move to higher potentials). This is illustrated in Figures 8a-8c which show positive J-V obtained in a high-current ion implanter (8) using special CHARM-2 wafers employing different area charge-collecting electrodes connected to the substrate.



(a)



(b)



(c)

Figure 8. Positive J-V plots recorded in the center of a bare wafer with different areas of charge-collecting electrodes connected to the substrate: (a) Intermediate charge collection area - the vertical line at ~ 2.4 V indicates non-responding sensors, and should be ignored; (b) Small charge collection area connected to the substrate; (c) Minimum charge collection area - the vertical line at ~ 2.4 V indicates non-responding sensors, and should be ignored.

Similar results have been obtained in plasma equipment (7). A quantitative model for this phenomenon does not exist, either.

## WAFER-PLASMA INTERACTIONS

Accurate characterization of charging sources, although very important for equipment and process optimization, is only “one side of the coin”. The “other side”, which determines the extent of device damage, is the interaction of the charging source with the wafer. Here, charging data must be properly interpreted and device physics must be accurately taken into account, as discussed in the following examples.

### Potentials vs. Currents

Frequently, high potentials are recorded in plasma and ion-beam wafer processing equipment. Although typically a cause of concern, just how important are they? To answer this, it is important to consider how charging causes damage. Gate oxide damage occurs when *current* flows through the gate oxide, creating and/or filling charge traps (1). Consequently, potentials are important only to the extent that they may cause current flow through the gate oxide. However, when gate oxide conducts current, it clamps the voltage across it to the value dictated by its current-voltage characteristic. This is illustrated in Figure 9, which shows how a charging source which exhibits higher potentials<sup>5</sup> but lower current density (Process 2; low density plasma) causes less oxide current and is less damaging than a charging source which exhibits lower potentials but higher current density (Process 1; high-density plasma). Figure 9 makes it clear that it is much more important to focus on charging currents than on charging potentials.

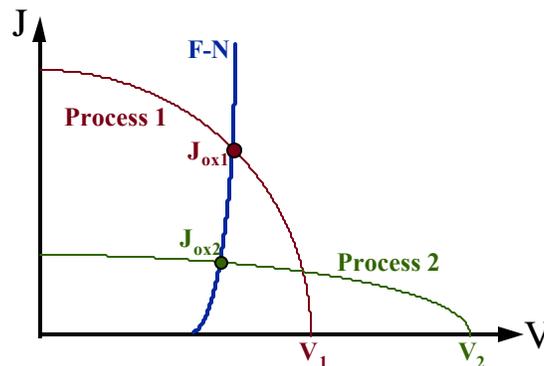


Figure 9. The intersection of the oxide J-V characteristics (F-N plot) with the plasma J-V characteristics (Process 1; Process 2) determines the oxide current density,  $J_{ox}$ , which is responsible for gate oxide damage. Note that damage is independent of the values of peak potentials ( $V_1$ ;  $V_2$ ), since the oxide F-N characteristic clamps the gate oxide voltage to a much lower value than  $V_1$  or  $V_2$ .

<sup>5</sup> It should be noted that the values of potentials at  $J = 0$  represent the potentials measured by the potential sensors.

### Damage during Ion Implantation

Although positive charging would appear to be more damaging than negative charging during ion implantation due to its significantly higher current density, as shown in Figure 2a, the pulsed charging in high-current ion implanters<sup>6</sup> causes deep depletion of the substrate under the gate of n-channel devices and reverse-biases the n-wells under the p-channel devices (12). This divides the positive charging voltage between the gate oxide and the depletion region (or the n-well), thus lowering the voltage across the gate oxide. Consequently, reducing positive potentials to moderate levels in CMOS processing with the aid of “electron-showers” or plasma flood systems can completely eliminate damage from positive charging. However, as seen in Figure 2b, this comes at the expense of increased negative charging which accumulates the substrate under n-channel devices. In this case, the entire applied voltage appears across the gate oxide, causing oxide conduction and resultant damage. Consequently, over-flooding is more likely to cause damage to n-channel devices than under-flooding.

### Damage during Plasma Processing

With regard to charging, plasma processes differ from ion implantation in two significant ways. Although RF driven, charging currents in plasma processes are typically steady-state currents, not repeated transients as in the case of ion implants. In addition, plasma processes are accompanied by high levels of UV emissions [13], which reduce the protective effects of depletion layers and reverse-biased junctions<sup>7</sup>, and cause additional damage [14]. These two differences significantly modify the conclusions reached for ion implants.

Although damage to n-channel devices exposed to negative charging is unlikely to be significantly affected by UV, n-channel devices exposed to positive charging are affected by UV. Since UV generates electron-hole pairs in the silicon substrate, under steady-state charging the deep-depletion layer collapses due to the formation of an inversion layer under the gate. This increases the voltage across the gate oxide, thereby significantly increasing the probability of damage from positive charging. This is particularly true of high-density plasmas, where very high UV intensity and high positive charge fluxes are present. Consequently, in plasma equipment damage to n-channel devices can occur as a result of both negative and positive charging, and, therefore, can correlate to negative current density, positive current density, and UV intensity.

P-channel devices are affected by UV during both negative and positive charging. During negative charging, the deep-depletion region (which would form under the gate in pulsed-charging situations in the absence of UV) collapses in the presence of UV due to the formation of an inversion layer. This increases the voltage across the gate oxide, thereby significantly increasing the probability of damage from negative charging. In the case of positive charging, the protection offered by the reverse-biased n-well/substrate junction is disabled by junction leakage caused by UV. Consequently p-channel devices become more vulnerable to damage from negative and positive charging in the presence of UV. Damage might thus correlate to negative current density, positive current density, and UV intensity.

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<sup>6</sup> Due to wheel rotation past the beam.

<sup>7</sup> Many down-stream ashers do not expose wafers to UV emissions.

In addition, UV allows oxides to conduct (13), thereby providing another mechanism for device damage. Indeed, device data exists which clearly implicates UV in device damage observed in an oxide etcher (15). Moreover, UV-assisted oxide conduction is the cause of charging damage in oxide depositions (5). As a result of UV emissions and the higher current densities present in high density plasma equipment, HDP equipment can be much more damaging than high current ion implanters.

#### “Anomalous” Effects

The “anomalous effects”, namely the enhancement of positive charging in the presence of large (non-shading) features, and the modulation of charging potentials and J-V plots due to connection of charge collecting antennas to substrate, are troublesome since they undermine confidence in steps taken to avoid charging damage. Product charging damage is typically avoided by employing design rules which limit the size of charge collecting “antennas” connected to transistor gates. These design rules are formulated on the basis of damage data obtained from test chip structures. However, as the data presented here clearly shows, the damage to test structures will vary depending on the resist mask and test chip layout. Without a theoretical underpinning of these “anomalous” effects, we cannot be sure if the design rules are sufficient to prevent damage, or if they are unnecessarily restrictive. Both of these effects deserve further investigation.

#### ACKNOWLEDGMENTS

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