

Influence of Photoresist on Wafer Charging During High Current Arsenic Implant

Wes Lukaszek
Wafer Charging Monitors, Inc.
127 Marine Road
Woodside, CA 94062 USA

S. Reno and R. Bammi
National Semiconductor
3333 West 9000 South
West Jordan, Utah 84088 USA

Abstract - Surface-substrate potentials and charge fluxes observed during a high-current Arsenic implant on a wafer half-covered with photoresist were quantified using a CHARM[®]-2 charging monitor wafer¹. High negative potentials were observed on the bare portion of the wafer, while high positive potentials were observed on the photoresist-covered portion of the wafer. Substantially enhanced positive charge-flux was observed near the resist edge, on the bare side of the wafer. A model is proposed to explain these phenomena.

I. Introduction

Differences in charging on bare vs. photoresist-covered portions of wafers undergoing high-current ion implants have been observed since the advent of high-current ion implanters [1]. However, since the vehicles employed to study this phenomenon have typically been device-based test patterns which can only record the device damage resulting from the implant, the explanations for this phenomenon have been inferred from device damage statistics. This approach, although widely employed in the IC industry, is subject to a variety of influences, such as gate oxide defects, test pattern layout details, etc., which can substantially affect the sensitivity and spatial response of these vehicles. Moreover, due to gate oxide defects, device-based results are noisy, and usually do not provide adequate spatial resolution of the change in the charging characteristics as function of position on the wafer. In addition, the driving forces behind the damage - the wafer surface-substrate potentials and charge fluxes impinging on the wafer - cannot be determined from such measurements, although their knowledge is essential to formulation of sound, physics-based charging models.

Due to these shortcomings, CHARM[®]-2 wafers, whose response is independent of process variations and is calibrated to provide the magnitudes and polarities of wafer surface-substrate potentials and charge-fluxes impinging on a wafer, have been chosen to investigate the charging differences between bare vs. photoresist portions of a wafer undergoing Arsenic ion implant. The CHARM[®]-2 wafer used in this experiment was implanted in a NV 10/80 ion

implanter at an energy of 80 KeV and dose of $4e15$. The beam current of 3.8 mA was neutralized with an electron shower such that the average disc current was -4 mA. The right half of the CHARM[®]-2 wafer was covered with photoresist, while the left half was bare.

The following briefly describe the capabilities of the CHARM[®]-2 technique, and the results obtained from the CHARM[®]-2 wafer. A model is proposed to explain the results.

II. Description of CHARM[®]-2

The 150mm CHARM[®]-2 wafers used in this experiment contain 188 sites (8 mm x 8 mm die) populated with EEPROM-based, calibrated, polarity-sensitive sensors of wafer surface-substrate potentials, net charge flux, and UV dose [2].

The CHARM[®]-2 potential sensors are implemented by connecting a charge collection electrode (CCE) on the surface of the wafer to the control-gate of an EEPROM transistor, as shown in Fig. 1. The CHARM[®]-2 potential sensors thus resemble the widely used "antenna" devices, employing gate oxide capacitors or transistors, except that in CHARM[®]-2 the sensing element is not gate oxide, but a EEPROM transistor, whose threshold voltage is changed by the voltage developed on the CCE. The post-experiment threshold voltage of the EEPROM transistor is converted, with the use of the V_g - V_t characteristics of the EEPROM transistor, into wafer surface-substrate potentials [2]. The potential sensors are implemented in pairs, where one sensor is used to measure negative potentials and the second sensor is used to measure positive potentials [2].

The CHARM[®]-2 charge-flux sensors are implemented by adding current-sensing resistors between the CCE and the substrate of the potential sensors, as shown in Fig. 2. In this configuration, the EEPROM transistor is used to measure the voltage across the current-sensing resistor, from which the current density may be determined. The charge-flux sensors are also implemented in pairs, where one sensor is used to measure negative charge-flux and the second sensor is used to measure positive charge-flux.

¹ CHARM[®] is a registered trademark of Wafer Charging Monitors, Inc.

positive charging on the photoresist-covered portion of the wafer is obtained from the positive J-V plots shown in Fig. 6, which shows the J-V plots for all die in row 9 (numbered from the bottom of the wafer). The vertical asymptote near 3V represents non-responding sensors for die in the bare-portion of the wafer⁴, while the modest response shown in curves 9-15, illustrated in expanded form in Fig. 7, represents the response for die in the photoresist-covered portion of the wafer. The highly irregular J-V plot obtained in die 7 (numbered from the left side of the wafer), next to the resist edge, is not an artifact but rather represents two separate J-V plots obtained from the two clusters of charge-flux sensors located 4 mm apart, indicating a rapid spatial variation in the charging environment. (The CHARM[®]-2 charge-flux sensors are located in two clusters, with the “odd” numbered sensors in the left group, and the “even” numbered sensors located in the right group. Since the plotting routine connects the data from the sensors in consecutive order, a “zig-zag” pattern occurs when the response from the two groups is substantially different, which occurs in those regions of the wafer where the charging environment varies rapidly as function of position.) This behavior was confirmed to be reproducible for all die in column 7. In the positive J-V plot for die 7, the group of charge-flux sensors closer to the resist edge shows the larger positive current densities.

The negative J-V plots exhibit complementary, though somewhat less striking behavior, as shown in Fig. 8 and 9, which show the negative J-V plots for die 6, 9, and 10 (die locations on both sides of the bare wafer-photoresist transition region), and the negative J-V plots for die 7 and 8 (die locations in the immediate neighborhood of the transition region), respectively. As shown in Fig. 8, die 6, 9, and 10, and all other die to the left of die 6 and to the right of die 10 (not shown for clarity) show similar behavior⁵, indicating similar negative charging characteristics away from the bare wafer-photoresist transition region. However, it should be observed that die 9, which is closer to the transition region, exhibits lower magnitude of negative charge-flux than die 10, which is 8mm farther from the transition region. The negative J-V plots for die near the bare wafer-photoresist transition region indicate considerably different behavior, as shown in Fig. 9. In particular, the J-V plot for die 7 shows a “zig-zag” pattern similar to the positive J-V plot, although in the negative J-V plot the group of charge-flux sensors closer to the resist edge records lower magnitude of negative current densities than the group of sensors farther from the resist edge. The negative J-V plot

for die 8 shows the vertical asymptote characteristic of non-response, indicating that this resist-covered die immediately near the resist edge suffers from a shortage of negative charge-flux.

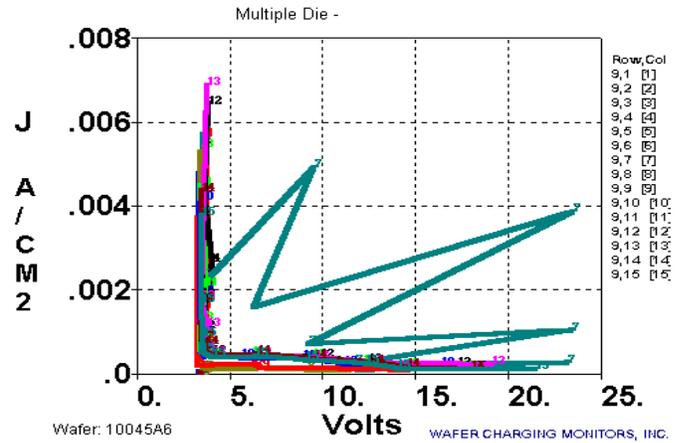


Figure 6. Positive J-V plots for all die in row 9.

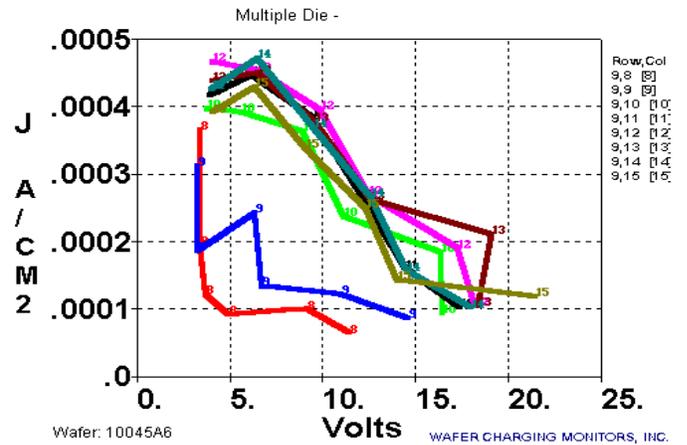
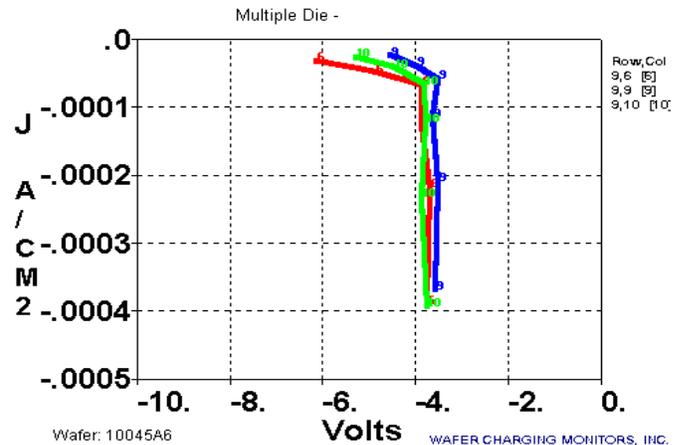


Figure 7. Positive J-V plots for die in row 9, on the photoresist-covered portion of the wafer.



⁴ The upper-limit voltage representing the no-response condition, when divided by decreasing values of current sensing resistors gives rise to a vertical asymptote - an artifact of the data conversion procedure.

⁵ The asymptote near -3.5V once again represents the no-response condition, and is an artifact of the data conversion procedure.

Figure 8. Negative J-V plots for die 6, 9, and 10 in row 9, illustrating similar behavior of the negative charging characteristics on either side of the bare wafer-photos resist transition region.

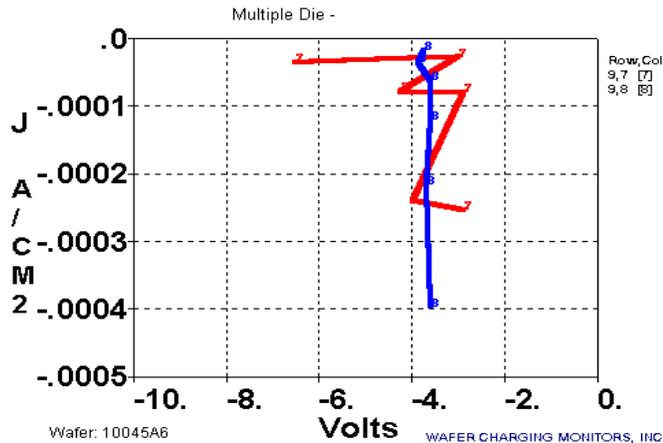


Figure 9. Negative J-V plots for die 7 and 8 in row 9, illustrating the difference in behavior of the negative charging characteristics in the neighborhood of the bare wafer-photos resist transition region.

IV. The Resist-Mediated Charging Model

The phenomena recorded in Fig. 4-9 may be qualitatively accounted for by a model which postulates that the positively charged photoresist attracts the flood electrons and the secondary electrons generated by the beam, thereby increasing the net positive charge-flux, and decreasing net negative charge-flux on the bare side of the wafer near the resist edge. Although it is not possible to test the model quantitatively due to lack of fundamental information such as beam size, plasma density near the wafer, etc., the model appears to be self-consistent. In particular, since the environment around the wafer is a plasma [7], the distance over which the photoresist will exert its influence will be limited by Debye screening. This is supported by the positive J-V plots which clearly indicate differences in J-V characteristics only in the region nearest the photoresist edge. Within this distance of a few Debye lengths, the resist will exert the greatest influence on regions nearest to it. This is also supported by the J-V plots.

On the photoresist side of the wafer, this model suggests that, due to the collected electrons, the positive charge-flux will be reduced most near the resist edge, but will increase with increasing distance from the resist edge. This is also supported by the J-V plots in Fig. 7 which show lowest positive charge-flux near the resist edge (die 8), with almost complete recovery in die 10. Moreover, the reduced positive charge-flux in die 8 is accompanied by reduced negative charge-flux (which neutralized the positive charge flux), as shown in Fig. 9. As the positive charge-flux recovers to a

constant level in die 10-15, shown in Fig. 7, so does the negative charge-flux, as shown in Fig. 9.

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