Use of EEPROM-based Sensors in Investigating Physical Mechanisms Responsible for Charging Damage

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ABSTRACT

Wafer charging damage in IC process equipment is the result of complex interactions between the wafer environment and the wafer. EEPROM-based sensors have been used recently to quantify the UV and charging characteristics of process tools, and to examine the interactions between the wafer environment and the wafer. This paper discusses these topics, relates them to charging damage, and illustrates them with examples from experiments performed in different process tools. [*Keywords*: charging damage, charging monitors, ion implantation, plasma, CHARM-2]

INTRODUCTION

Product charging damage in IC processing equipment has been a recurring problem in IC manufacturing for nearly two decades. Although significant effort is devoted by equipment makers and IC manufacturers to control wafer charging, new charging mechanisms emerge as equipment designs change and as IC technologies are scaled for higher performance. Consequently, understanding charging damage in contemporary tools and technologies is an on-going challenge. This paper reviews the current state of understanding, and the contributions made to it through the use of EEPROM-based charging monitors. Examples from experiments conducted in different process tools are presented to illustrate the various charging mechanisms, and the interactions between charging sources and device structures which determine the extent of device damage.

FUNDAMENTALS OF CHARGING DAMAGE

Although understanding damage to insulators during wafer processing can be complicated by many details, the underlying concepts are relatively simple. Damage to thin insulators (gate oxides) sandwiched between a conductive substrate and isolated conductive electrodes on the surface of a wafer (gates) occurs due to *current flow* through the insulator, driven by a potential difference between the surface electrodes and the substrate. [1] When the substrate is electrically floating, differences in potential between electrodes located in different portions of a wafer can cause current flow from one set of electrodes to the other through the insulators and the substrate.

The magnitude of the oxide current density, J_{ox}, responsible for gate oxide damage, is determined at the intersection of the charging source J-V plot with the J-V characteristic of the gate oxide (F-N plot)[1], as illustrated in Figure 1 for two different processes. Note that J_{ox}, (and, therefore, magnitude of damage) is **independent** of the values of peak potentials (V_1; V_2) developed by a process, since the oxide F-N characteristic clamps the gate oxide voltage to values lower than V_1 or V_2. Consequently, a charging source which exhibits higher potentials but lower current density (Process 2) causes less oxide current (and is less damaging) than a charging source which exhibits lower potentials but higher current density (Process 1). If the process J-V plot does not intersect the gate oxide J-V plot, the voltage across the oxide will reach the peak potential developed by the process, but since $J_{ox} = 0$, the oxide will not be damaged.

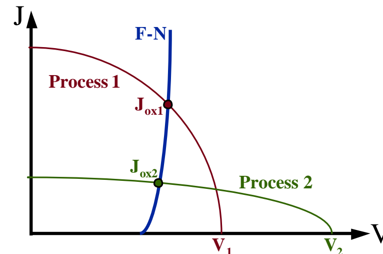


Figure 1. The magnitude of the oxide current density, J_{ox}, is determined at the intersection of the process J-V plot (illustrated here for two different processes) and the J-V characteristic of the gate oxide (F-N plot). The voltage axis represents the wafer surface-substrate potential.

This procedure for determining J_{ox} can be performed only if the charging characteristics of a process tool are obtained with a probe implemented on a wafer, so the process current density can be measured as a function of the wafer surface-substrate potential, analogous to the gate oxide J-V plot.

CHARGING MONITOR

The CHARM®-2 monitor, implemented as a monolithic silicon wafer populated with microscopic, EEPROM-based potential, charge-flux, and UV sensors, was designed precisely for this purpose. [2] Because it is self-contained, and does not require connections to anything else, the CHARM®-2 monitor wafer can be used in any wafer processing tool[2].

The CHARM®-2 potential sensors are implemented by connecting a charge collection electrode (CCE) on the surface of the wafer to the control-gate of an EEPROM transistor, as shown in Figure 2a. The potential sensors are calibrated to measure peak surface-substrate potential in volts. Separate sensors are used to measure positive potentials and negative potentials.

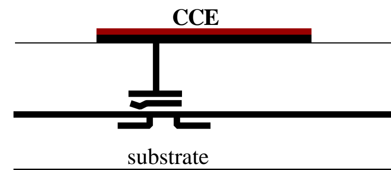


Figure 2a. CHARM®-2 potential sensor.

The charge-flux sensors are implemented by adding current-sensing resistors between the CCE and the substrate, as shown Figure 2b. In this configuration, EEPROM transistors measure the voltage

[1] Assuming an "antenna ratio" of one. Otherwise, the process J-V values should be multiplied by the antenna ratio.

[2] Provided the temperature is less than 430 ^{o}C.

across the current-sensing resistors, from which current density is calculated. The charge-flux sensors are calibrated to measure the net charge-flux in A/cm^2. Separate sensors are used to measure positive charge-flux and negative charge-flux. Since one sensor provides a single point in the J-V plane, data from many sensors (each with a different value resistor, R) are used to construct the positive and negative J-V characteristics of the charging source.

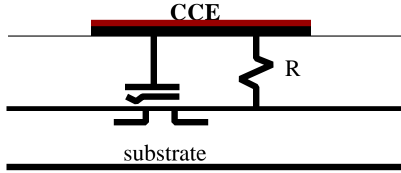


Figure 2b. CHARM®-2 charge-flux sensor.

The UV sensors are similar in construction to charge-flux sensors, except that the resistor values and the CCE areas are deliberately very small. The small CCE areas minimize the collected charge which, in conjunction with low value current-shunting resistors, ensures that electrostatic charging does not disturb the response of the UV sensors.

Conversely, the potential and charge-flux sensors are heavily shielded against UV to ensure that UV does not affect their response. Since the potentials, charge-fluxes, and UV intensity are measured with separate sensors, it is possible to distinguish UV effects from electrostatic charging effects. The use of separate sensors to measure positive and negative charging also allows measurement of both polarity charging characteristics at the same location, which occurs in ion implanters [3], as well as other tools when opposite polarity transients are present.

The remainder of this paper will discuss charging phenomena in ion- and plasma-based process tools, and their interaction with the wafer. The observations will be illustrated with data from experiments performed with the CHARM®-2 monitors.

CHARGING IN ION INPLANTATION

When devices are under the beam in a high-current ion implanter, they are exposed to positive charging from the high-energy ion beam, from "slow" ions (from ionized background gases or from the plasma used for charge neutralization), and from secondary electrons emitted from the surface of the wafer due to ion impact. They are also exposed to negative charging from the "electron shower" or plasma electrons from the plasma flood system used to neutralize positive charging. Therefore, the **net** positive charging when devices are under the beam is the sum of the positive and negative charging just described. On the other hand, when devices are outside the beam, they experience only negative charging from the "electron shower", or from the plasma flood system. [3] A quantitative formulation of this model, based on CHARM-2 data, has been used to optimize the charging performance of plasma charge-control systems. [4]

The balance between positive and negative charging, controlled by the "electron shower" or a plasma flood system, is illustrated in Figures 3a and 3b. Higher positive charging in die (11,21), curve 21, shown in Figure 3a, is associated with lower negative charging, shown in Figure 3b. Conversely, lower positive charging in die (11,14), curve 14, is associated with higher negative charging. (In this case, the spatially non-uniform output of the charge neutralization system gave rise to spatially non-uniform positive and negative charging.)

It should be noted that positive current densities in high-current ion implanters are typically ~ 100 times greater than negative current densities, which makes positive charging potentially much more destructive than negative charging. This was, indeed, the case with early generation high-current ion implanters.

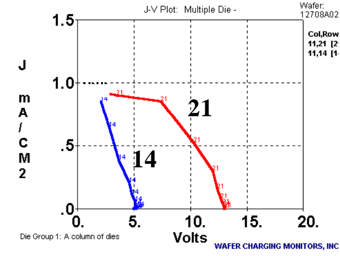


Figure 3a. Positive J-V plots recorded at two different locations on a wafer during a high-current ion implant.

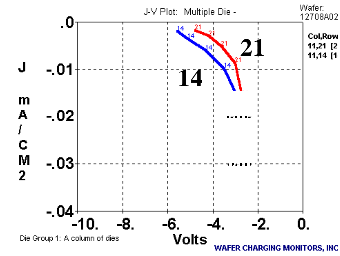


Figure 3b. Negative J-V plots recorded at the same locations on the same wafer during a high-current ion implant.

By increasing the output of the "electron shower" or a plasma flood system, the positive J-V plots may be shifted to low voltages, such that the positive J-V plots do not intersect the gate oxide J-V plot, thereby suppressing damage from positive charging. However, as seen in Figure 3b, this also shifts the negative J-V plots to higher voltages, causing them to intersect the oxide J-V plot at higher values of J_{ox}, thereby creating more damage from negative charging[3]. Due to the significantly lower current densities associated with negative charging, this is still a very desirable trade-off. It allows contemporary high-current ion implanters to operate at their rated output (which was not possible with early generation high-current machines) because the low level of damage from negative charging can be completely annealed out during the high-temperature implant activation anneal.

Avoiding damage during high-current implants thus involves suppressing positive charging and minimizing negative charging, which requires optimum set-up of the "electron shower" or the plasma flood system. To optimize these settings, it is important to take into account that charging events in high-current implanters occur as alternating polarity pulses of very short duration (~ 1ms). The short duration positive pulse causes deep depletion of the substrate under the gate of N-channel devices, and reverse-biases the N-wells under the P-channel devices. This makes both N-channel and P-channel devices less vulnerable to damage from positive charging because the positive voltage becomes divided between the gate oxide and the depletion region (or the N-well), thus lowering the voltage across the gate oxide[4]. Consequently, it is sufficient to

[3] Peak negative potentials in high-current ion implanters are typically high. Consequently, some damage from negative charging is unavoidable.

[4] This has the equivalent effect of shifting the gate oxide J-V plot in Figure 1 to a higher voltage by the amount of the voltage drop across the depletion region, or the reverse-biased junction.

reduce positive potentials only to moderate levels[5] to completely eliminate damage from positive charging.

This is a very beneficial effect, because any additional reduction in positive charging would come at the expense of increased negative charging. Since the N-channel devices are unprotected, because negative charging accumulates the substrate under N-channel devices and causes the entire negative voltage to appear across the gate oxide, any increase in negative charging would lead to a direct increase in damage to N-channel devices. The P-channel transistors are less vulnerable to negative charging, because they are protected by the N-well depletion layer.

This behavior was confirmed in experiments which compared CHARM-2 data vs. damage to SPIDER-MEM transistors during high-current ion implants. [5] Damage to N-channel transistors correlated **only** to negative current density, as shown in Figure 4. This is contrary to the (still popular) belief that device damage in high-current implanters is due to positive charging – an explanation that was valid for the early generation machines which lacked adequate charge-control systems, but which is not appropriate for contemporary high-current implanters equipped with modern charge-control systems.

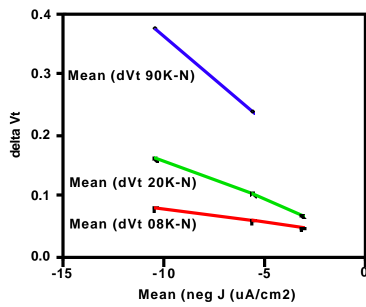


Figure 4. Threshold voltage shift due to ion implant damage of 45? gate oxide N-channel transistors vs. negative current density at –5V.

The preceding discussion suggests a straightforward method for optimizing the charge-control system settings of high-current ion implanters to minimize charging damage. The charge-control system could be adjusted to move the positive J-V plots to voltages slightly lower than the combined voltage drop across the P-well depletion layer (or the breakdown voltage of the N-well-to-substrate junction) and the oxide breakdown voltage. This would prevent damage from positive charging, while minimizing negative charging to minimize damage to N-channel transistors.

Unfortunately, things are more complicated due to the presence of resist patterns used for S/D implants. Resist patterns which cover most of the wafer (dark-field) significantly increase the positive charging effects. This was initially attributed to the collection of positive charge by the carbonized resist, and its subsequent conduction to devices in the resist holes. [6] However, CHARM-2 experiments using a resist mask designed to emulate CMOS layouts proved this hypothesis to be incorrect. Positive J-V plots obtained in patterns where the resist edge touched the charge-collection-electrodes (CCEs) were indistinguishable from those obtained in patterns where the resist edge did not touch the CCEs, indicating that the resist did not convey any additional current into the resist holes. However, the positive potentials recorded in the resist holes were higher than on bare CHARM-2 wafers, and the positive current densities recorded in the resist holes were significantly higher than those recorded with bare CHARM-2 wafers. [7] Negative charging results also did not support the carbonized resist conduction hypothesis. Highest negative potentials were observed on CCEs which did not touch the resist on the field oxide.

Although both resist out-gassing and higher secondary electron emission coefficient for photoresist were proposed as possible causes of these effects, and although some of the results are consistent with them, they do not explain all of the observed data. A series of recent experiments uncovered yet another variable which may be responsible for, or at least contribute to, this behavior. When the area of charge-collecting electrodes connected to the substrate decreases, the wafer potentials increase (and J-V plots shift to higher potentials). This is illustrated in Figures 5a-5c which show positive J-V obtained in a high-current ion implanter [8] using special CHARM-2 wafers employing different area charge-collecting electrodes connected to the substrate. It is possible that the presence of resist on the surface of the wafer elevated the positive potentials and current densities by reducing the total area of charge collecting electrodes connected to the substrate, causing the effect illustrated in Figures 5a-5c. A quantitative model for this “substrate-antenna” phenomenon does not exist. Its implications are discussed later in this paper under "Implications of Anomalous Effects."

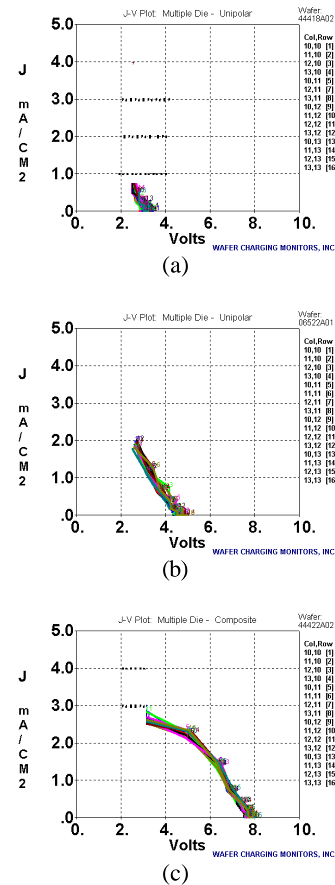


Figure 5. Positive J-V plots recorded during high-current ion implant in the center of bare wafers with different areas of charge-collecting electrodes connected to the substrate: (a) Large charge collection area; (b) Intermediate charge collection area; (c) Small charge collection area.

CHARGING IN PLASMA TOOLS

During wafer processing in plasma tools, **global** (wafer scale) potential differences are caused by global non-uniformities in plasma density and/or electron temperature. [9] This causes an imbalance

[5] Determined primarily by the avalanche breakdown of the P-well, and the N-well-to-substrate junction.

between ion and electron fluxes in different regions of a wafer, which gives rise to different surface-substrate potentials over large areas of the wafer. (As will be shown later, highly localized charging events scattered over a large area of the wafer are also sometimes observed in plasma equipment.) Charging damage in processes where the electrodes are entirely exposed, such as resist stripping is typically associated with global variations in surface charging. [10] Likewise, charging damage during oxide depositions is associated with global variations in surface charging [11], or a combination of surface charging and UV. [12]

Even in uniform plasmas, highly localized charging due to **local** imbalance in ion and electron fluxes associated with holes-in-insulator topographical features may cause gate oxide damage. This localized charging, called "electron shading" [13] is due to negative charging of the insulator (e. g. resist) which prevents low energy electrons from reaching the bottom of the hole to neutralize the positive ion flux, thereby causing net positive charging at the bottom of the hole. The magnitude of this fundamental effect increases with increasing aspect (height/width) ratio. Charging damage in etching processes is caused by a combination of both global and localized charging. As will be shown later, the localized charging caused by "electron shading" is superimposed on the global charging effects.

As in the case of ion implantation, another variable which influences the magnitude of the potentials and currents experienced by device structures in plasma-based process tools is the area of charge collecting electrodes (antennas) connected to the substrate. [14, 15]

As regards interaction with device structures and charging damage, plasma processes differ from ion implantation in two significant ways. Although RF driven, charging currents in plasma processes are typically steady-state currents, not repeated transients as in the case of ion implants. In addition, plasma processes are accompanied by high levels of UV emissions [16], which reduce the protective effects of depletion layers and reverse-biased junctions[6], and cause additional damage [17]. These two differences significantly modify the observations for plasmas compared to those made earlier for ion implants.

Although damage to n-channel devices exposed to negative charging is unlikely to be significantly affected by UV (except in oxide depositions), n-channel devices exposed to positive charging are affected by UV. Since UV generates electron-hole pairs in the silicon substrate, under steady-state charging the deep-depletion layer (which would form under the gate in pulsed-charging situations in the absence of UV) collapses due to the formation of an inversion layer under the gate. This increases the voltage across the gate oxide, thereby increasing the probability of damage from positive charging. This is particularly true of high-density plasmas, where **very high** UV intensity and high positive charge-fluxes are present. Consequently, in plasma tools damage to n-channel devices can occur as a result of both negative and positive charging, and, therefore, can correlate to negative current density, positive current density, and UV intensity.

P-channel devices are also affected by UV during both negative and positive charging. During negative charging, the deep-depletion region collapses in the presence of UV due to the formation of an inversion layer. This increases the voltage across the gate oxide, thereby increasing the probability of damage from negative charging. In the case of positive charging, the protection offered by the reverse-biased n-well/substrate junction is reduced by junction leakage caused by UV. Consequently, p-channel devices become more vulnerable to damage from both negative and positive charging in the presence of UV. Damage might thus correlate to negative current density, positive current density, and UV intensity.

[6] Many down-stream ashers do not expose wafers to UV emissions.

In addition, UV allows oxides to conduct, thereby providing another mechanism for device damage. [16] Indeed, UV-assisted oxide conduction can be the cause of charging damage in oxide depositions. [12] The interaction of surface charging and UV in etchers can also cause difficult-to-understand charge-storage problems in IC products that contain EPROM transistors. [18,19]

Due to UV emissions and the higher current densities present in high-density plasma equipment, HDP equipment can be **much more** damaging than high-current ion implanters. This, and the other points made previously, will be illustrated in the following examples.

Charging in Non-Uniform High-density Plasma

A typical spatial relationship between positive charging, negative charging, and UV intensity in a "simple", high-density plasma (HDP) is shown in Figures 6a-6c. In this case, the positive potentials are highest around the perimeter of the wafer, whereas negative potentials are highest in the center of the wafer. The high positive potentials around the perimeter of the wafer indicate a region of higher plasma density, which is consistent with lower UV emissions[7], as shown in Figure 6c.

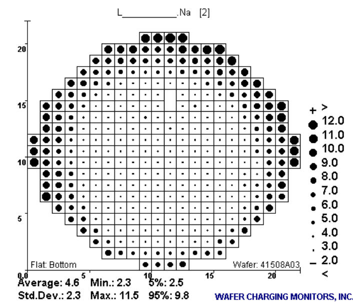


Figure 6a. Positive potentials in a HDP.

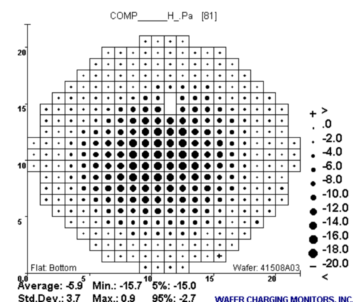


Figure 6b. Negative potentials in a HDP.

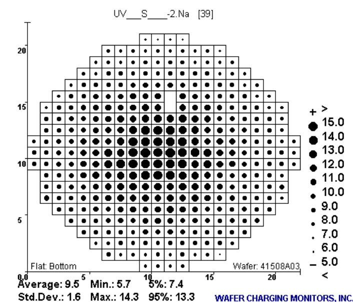


Figure 6c. Relative UV intensity in a HDP.

[7] In HDP, higher plasma density leads to **lower** UV emissions, whereas the opposite is true for low-density plasmas.

(The complementary relationship between the potential wafer maps and the UV wafer map makes it easy to confuse the response from UV with the response from charging when using the contactless techniques which employ oxidized wafers as charging monitors.) [20] The high plasma density causes positive current to enter the wafer around the perimeter[8], as shown in Figure 6d, and leave through the center of the wafer, as shown in Figure 6e.

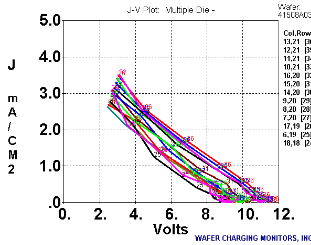


Figure 6d. Positive J-V plots in HDP from wafer perimeter.

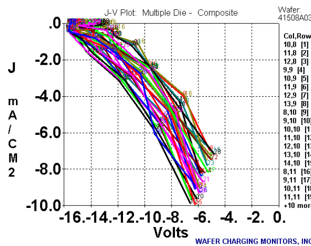


Figure 6e. Negative J-V plots in HDP from center of wafer.

The complementary behavior illustrated in Figures 6a-6e can take on many different forms. For example, gradient patterns are often observed where positive charging occurs on one side of the wafer and negative charging occurs on the opposite side of the wafer. [21]

Occasionally, plasma instabilities occur which cause highly localized charging scattered over a significant portion of the wafer, as illustrated in Figures 7a – 7c.

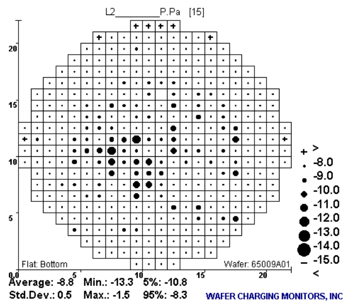


Figure 7a. Negative potentials recorded by a single sensor in a die.

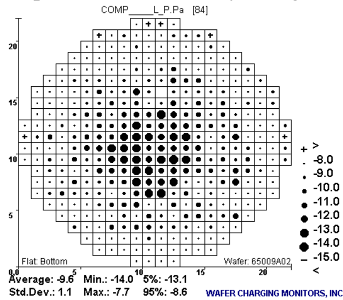


Figure 7b. Highest negative potentials recorded by one of four sensors in a die.

[8] Current is defined here as the flow of positive charge (EE sign convention).

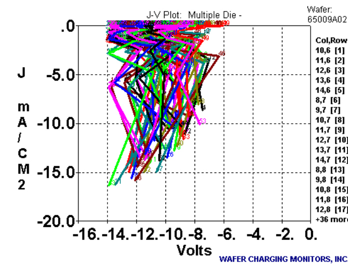


Figure 7c. Negative J-V recorded in the central portion of the wafer. (Sensors are saturated at ~ -14V, truncating the J-V plots.)

Figure 7a shows what appears to be random negative charging. However, when the maximum value from four identical sensors in each die is displayed, it becomes clear that charging was not random, and that the most intense activity occurred in the center of the wafer, as shown in Figure 7b. The irregular ("zig-zag") nature of the negative J-V plots (obtained by combining data from many sensors in each die), shown in Figure 7c, confirms that different sensors within the die experienced very different charging conditions. Because these sensors are only millimeters apart, this indicates that **very intense**, highly localized charging events occurred in the center of the wafer. [21]

Pattern-Induced Charging ("Electron Shading") in Uniform Plasma

The localized charging effect ("electron shading") caused by hole-in-insulator topographies is illustrated in Figures 8a, 8b, and 8c. Figure 8a is a wafer map of positive potentials obtained in a plasma oxide etcher using a bare wafer (no topography). The potentials are low and uniform over the entire wafer, indicating good plasma uniformity.

On the other hand, Figure 8b is a wafer map of positive potentials obtained in the same oxide etcher using a wafer covered with photoresist patterned with holes using electron-beam lithography. The elevated potentials in the different sites illustrate the effect of the twelve different designs, which used different size and number of holes in the resist over the charge-collection-electrodes.

Figure 8c illustrates the aspect-ratio dependence of the localized, topography-induced charging. Both peak potentials and current densities measured with the 0.3µm hole pattern are higher than those obtained for the 0.6µm hole pattern. [22]

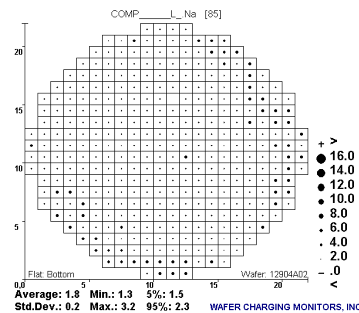


Figure 8a. Positive potentials in an oxide etcher recorded with a bare wafer.

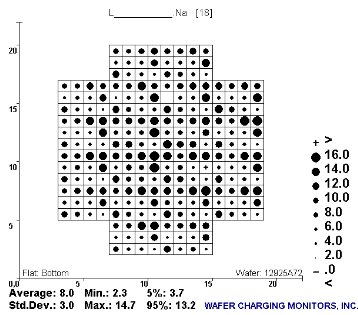


Figure 8b. Positive potentials in an oxide etcher recorded with a wafer covered with patterned resist.

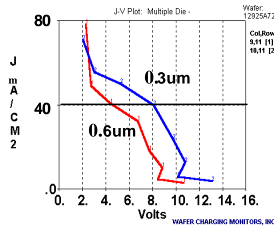


Figure 8c. Positive J-V in 0.6 µm and 0.3 µm resist holes measured in an oxide etcher.

"Electron Shading" in Non-Uniform Plasma

When patterned resist wafers are processed in a tool which exhibits plasma non-uniformity, the "electron shading" and the plasma non-uniformity effects add, as shown in Figures 9a–9d. Figures 9a and 9b show the positive potentials on a bare wafer and a resist-patterned wafer, respectively, in an oxide etcher. The plasma non-uniformity is evident in Figure 9a, where elevated positive potentials are recorded around the periphery of the wafer. However, the potential sensors under the 0.5 µm holes on the resist-patterned wafer, shown in Figure 9b, are **saturated** at ~ 14V due to the "electron shading" effect.

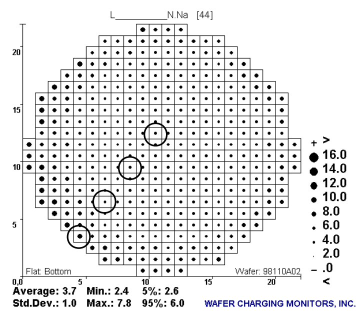


Figure 9a. Positive potentials on a bare wafer in a non-uniform plasma oxide etcher. J-V plots in Figure 9c come from circled die.

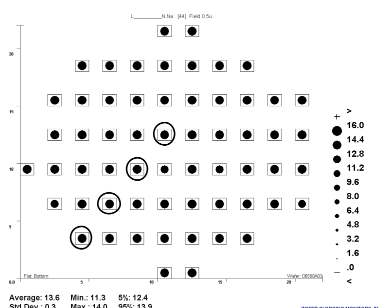


Figure 9b. Positive potentials in 0.5µm resist holes in a non-uniform plasma oxide etcher. J-V plots in Figure 9d come from circled die.

The same trend is evident in the positive J-V plots. Figures 9c and 9d show the positive J-V plots obtained in the same four (circled) die. On the bare wafer, the two edge-most die show a response (curves 1 and 2), while the other two die do not. (The vertical lines at ~ 2.7 V indicate no response.) The corresponding positive J-V plots obtained on the resist covered wafer are shown in Figure 9d, where J-V plots were recorded in all four die. The bottom two J-V plots come from the uniform plasma portion of the wafer, where no J-V plots were recorded on the bare wafer. They are due to the "electron shading" effect. Plot 2 comes from the inner portion of the wafer, where non-uniformity was minimally detected on the bare wafer. Plot 1 comes from the edge of the wafer, where **significant** non-uniformity was detected on the bare wafer. [23] The large increase in positive current density shown in plot 1 is the reason why damage to product, if any, always occurs in the region of plasma non-uniformity. It is also the reason why plasma non-uniformity must be eliminated to attain maximum yields and best reliability.

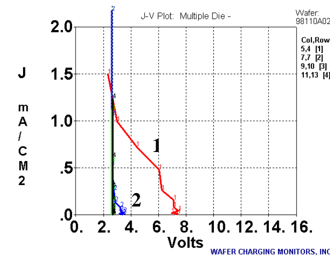


Figure 9c. Positive J-V on a bare wafer in an oxide etcher.

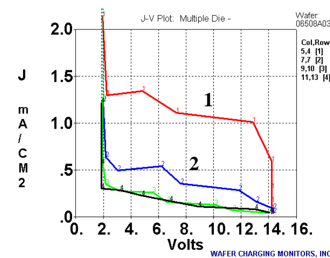


Figure 9d. Positive J-V recorded in 0.5 µm resist holes in an oxide etcher. (Sensors are saturated at ~ 14V, truncating the J-V plots.)

"Anomalous" Effects

The previous examples support the widely accepted plasma non-uniformity and the "electron shading" charging models. However, additional effects exist for which adequate models have not been established. Figures 10a-10d compare positive potentials and J-V plots obtained in an oxide etcher with a bare wafer vs. a wafer covered with photoresist patterned with a product via mask. [24] Plasma non-uniformity, evident in the positive potentials and J-V plots obtained with a bare wafer (Figures 10a and 10b, respectively) is significantly amplified by the presence of the patterned photoresist, as shown in Figures 10c and 10d, respectively.

In particular, the positive J-V plots shown in Figure 10d were obtained from uncovered sensor locations coinciding with the product mask 100um-wide scribe lanes. (The J-V plots are irregular due to misalignment of open areas in the product mask and the CHARM®-2 wafer layout.) The dramatic increase in positive potentials and current densities in these locations cannot be attributed to the "electron shading" effect because the aspect ratio is **much** too low). A quantitative model for this phenomenon does not exist, although it may be due to the same effect as shown in the following example.

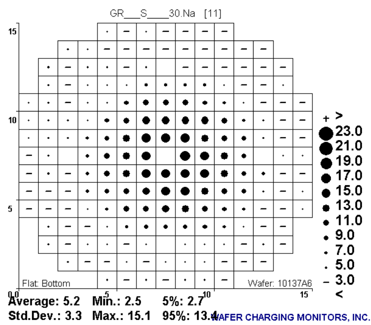


Figure 10a. Positive potentials on bare wafer in an oxide etcher.

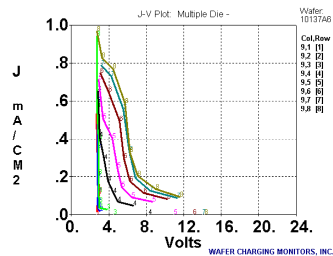


Figure 10b. Positive J-V plots obtained in a column of die through the center of a bare wafer in an oxide etcher.

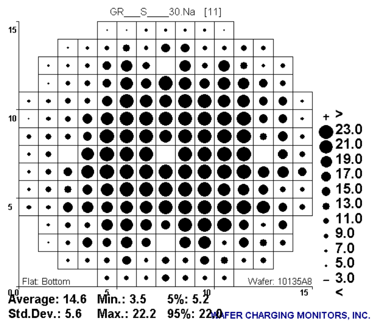


Figure 10c. Elevated positive potentials in an oxide etcher on a wafer covered with resist patterned with product via mask.

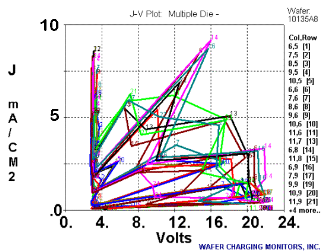
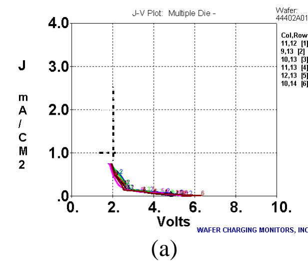
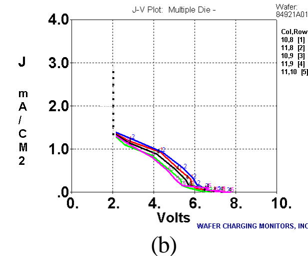


Figure 10d. Positive J-V plots obtained in an oxide etcher on a wafer covered with resist patterned with product via mask.

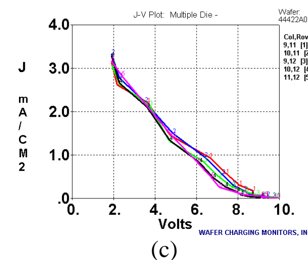
As previously discussed in connection with ion implantation, the area of antennas connected to the substrate can modulate wafer potentials and J-V plots in plasma tools. When the area of charge-collecting electrodes connected to the substrate decreases, the wafer potentials increase, and J-V plots shift to higher potentials. This is illustrated in Figures 11a-11c which show positive J-V plots obtained in an oxide etcher using special CHARM-2 wafers employing different area charge-collecting electrodes connected to the substrate. [15] A quantitative model for this phenomenon does not exist, although it is consistent with a model involving electrical loading of the plasma by the wafer – the less loading, the higher the peak values.



(a)



(b)



(c)

Figure 11. Positive J-V plots recorded in the center of bare wafers with different area charge-collecting electrodes connected to the substrate: (a) Large charge collection area; (b) Intermediate charge collection area; (c) Small charge collection area.

Implications of "Anomalous Effects"

The "anomalous effects", namely the enhancement of positive charging in the presence of large (non-shading) resist features, and the modulation of charging potentials and J-V plots due to connection of charge collecting antennas to substrate (which may be one and the same), are troublesome since they undermine confidence in steps taken to avoid charging damage. They indicate that the magnitude of surface-substrate potentials experienced by device structures arises from the interaction between the **entire** wafer and the process environment. Structures of interest are **not** the only ones responsible for the observed response. Their neighbors also exert an influence due to their connections to the substrate.

Product charging damage is typically avoided by employing design rules that limit the size of charge collecting "antennas" connected to transistor gates. These design rules are formulated on the basis of damage data obtained from test chip structures. However, as the data presented in this paper shows, the damage to test structures will vary depending on the resist mask and test chip layout. Without a theoretical underpinning of these "anomalous" effects, we cannot be sure if the design rules are appropriate to prevent damage, or if they are unnecessarily restrictive.

The examples presented in this paper suggest that charging results obtained with **identical** structures embedded in different test chips (or products) may differ **significantly**, due to unknown influence of other test structures (including scribe lane structures). [8,14,15] In view of this, different products (using identical design rules) may experience different charging stress under identical process conditions due to layout differences.

Of course, these results do not imply that test vehicles and the information derived from them are useless. On the contrary, since virtually all charging-reduction work in manufacturing involves relative comparisons between different tools or different processes, charging monitors can provide very useful information, provided that the data used to make the comparisons come from the **same** monitor. And as long as the monitor employed measures all variables relevant to damage, a reduction in charging-related parameters observed with such a monitor will reduce product damage. It must be kept in mind, however, that **direct comparisons** between different test vehicles, or test vehicles and product, **must take device physics into account** and should be done with caution. In particular, the design of test vehicles used to develop product antenna design rules needs to consider the impact of antenna areas connected to the **substrate** on **gate** antenna design rules. Due to the importance of gate antenna design rules for product yield and reliability, these "anomalous effects" deserve further investigation.

SUMMARY

Due to their ability to measure surface-substrate potentials, charge-fluxes, and UV intensity, the CHARM-2 EEPROM-based charging monitors have been used by IC manufacturers, disc drive manufacturers [25], and process equipment manufacturers to quantify and study charging phenomena inside process tools. The examples presented in this paper attempted to illustrate some of their applications, and what can be learned about charging phenomena by using them. The use of EEPROM-based sensors has clarified misconceptions, and has contributed to our understanding of charging phenomena in process tools. It has also expanded our awareness of things we do not yet understand about charging phenomena in process tools. It is hoped that their continued application by the industry will clarify the remaining puzzles.

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