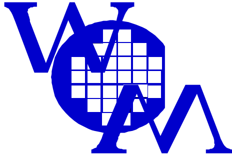

Wafer Charging Bulletin

Vol. 1, No. 1

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From the Editor ...

Welcome to the first issue of our bulletin, which will be devoted to the application of the CHARM®-2 technology to identify and eliminate sources of wafer charging damage, or UV damage, during wafer fabrication.

We will use this bulletin to disseminate knowledge and insights WCM has gained during the last three years while helping IC manufacturers and equipment makers solve their wafer charging problems. (We **will not** disclose confidential information.)

In future issues, we will discuss application procedures and success stories. We will try to dispel myths and misconceptions. And we will strive to provide you with helpful, accurate information about wafer charging in process equipment, and what can be done in a timely and cost-effective manner to minimize the damage it can cause to your products.

In addition to presenting what we've learned, we also want to make this bulletin a forum for the communication of experiences and insights of our customers. We welcome your suggestions, criticism, questions, and contributions.

In this issue, we'll discuss a topic which raises many questions - the use of equipment J-V characteristics, measured by probes on the surface of a wafer, for analyzing gate oxide damage.

We have chosen it as our first topic not only because J-V plots are a unique CHARM-2 capability, but because quantifying the J-V characteristics of process equipment is essential to understanding and prevention of gate oxide damage. Knowing surface-to-substrate potentials is not enough! In fact, it can be misleading, as demonstrated in the resist ashing example on page 4.

Process equipment J-V plots are most easily obtained with the CHARM-2 wafers and the ChargeMap™ data analysis and display software available from WCM. (WCM can also perform this analysis for you.) The ChargeMap software also generates wafer maps of UV intensity, and surface-to-substrate potentials, but the J-V plots are most important for predicting the probability of damage to product wafers.

Why are J-V plots important?

To answer this question, our first tutorial discusses the basic concepts of:
a) How gate oxide damage occurs
b) What the J-V plots show, and
c) How to use this information to predict the probability of gate oxide damage.

We hope that you find the following brief tutorial informative and useful. We would appreciate your feedback.

Please visit our web site, http://www.charm-2.com and send us your comments.

JV PLOTS AND DAMAGE PREDICTION

How Charging Damage Occurs

During wafer processing in a plasma or ion beam environment, a *net* charge (composed of both positive and negative charge) may collect on the surface of the wafer. As this *net* charge continues to accumulate, the surface-to-substrate potentials will rise. Transistor gate-to-substrate potentials will follow the surface-to-substrate potentials of the "antennas" to which the gates are electrically connected, until these potentials reach the conduction (~breakdown) voltage of the gate oxide.

Once the gate-to-substrate voltage, $\mathbf{V_{gs}}$, reaches the oxide conduction voltage, a tunneling current [also called the Fowler-Nordheim (F-N) current] will start to flow through the oxide ($\mathbf{J_{ox}}$ in Fig. 1). When this happens, V_{gs} will not increase appreciably, but oxide damage will begin to accumulate in proportion to the *magnitude of the F-N current*. The extent of damage will depend on the magnitude of the F-N current, J_{ox}, and the length of time, t_d, during which J_{ox} flows through the gate oxide.

Gate oxide characterization measurements show that **gate oxide damage is proportional to the *charge density absorbed* by the oxide** ($\mathbf{Q_{ox}}$ in Fig. 1). A fraction of this charge (in the range of 10^{-6} to 10^{-8} of $\mathbf{Q_{ox}}$) is trapped in the oxide. A measure of oxide robustness is a quantity called $\mathbf{Q_{bd}}$, defined as the total integrated charge that flows through the oxide such that enough charge is trapped to break down the oxide ($\mathbf{Q_{bd} = J_{ox} * t_{bd}}$ where $\mathbf{t_{bd}}$ is the time required to cause breakdown when Jox flows through the gate oxide). Q_{bd} is an empirical quantity for a given oxide in a given process. Good quality oxides exhibit Q_{bd}'s on the order of 10 coulombs/cm^2. If $Q_{ox} = J_{ox} * t_d$ approaches Q_{bd}, serious damage to the gate oxide occurs. However, onset of damage occurs when Q_{ox} reaches 0.1% to 1% of Q_{bd} **[1]**.

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It is important to remember that the amount of damage is *NOT* proportional to the surface-to-substrate potential, V_{ss}, but rather, to the magnitude of the oxide current, J_{ox}. (The Fowler-Nordheim characteristics and Qbd are both properties of the oxide, and are not related to the surface-to-substrate potential, V_{ss}.)

To summarize, because oxide damage is proportional to the charge trapped in the oxide, and the trapped charge is proportional to the magnitude of current flowing through the oxide, the greatest damage occurs in the region of highest charge flux that the charging source can supply at the gate oxide conduction (~ breakdown) voltage. **Maximum damage does not necessarily occur in the region of highest surface-to-substrate potential.**

It should also be recognized that damage to product gate oxides is not usually due to direct bombardment of the gate oxide by ions or photons, since the gate oxide is covered by the gate. **Physical damage due to ion bombardment and UV photon exposure at gate edges, as measured with contactless probe techniques, usually plays only a minor role in IC charging damage.**

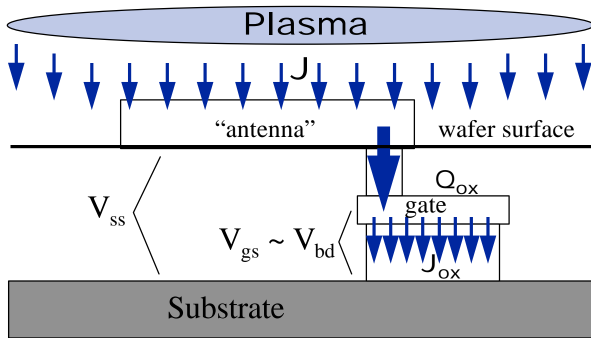

Figure 1. A view of a device after oxide conduction starts. (The diagram is not to scale, and is not a device cross-section. Its intent is only to convey the basic concepts described in this tutorial.)

The Source of Power that Drives Damage

We showed above that gate oxide damage is proportional to the current which flows through the oxide. Now we briefly discuss why high surface-to-substrate potentials do not necessarily result in high currents through the oxide.

Familiarity with Ohm's Law (I = V/R), which states that the higher the applied voltage, the greater the current, may lead one to believe that high surface-to-substrate potentials always result in high currents through oxides. However, Ohm's Law is true only for the current-voltage relationship of power-absorbing ***loads***, as long as the power required by the load does not approach the limits of the power source. This limit is commonly observed in batteries. As the current required from the battery is increased, the battery voltage decreases. For example, the lights dim (battery voltage decreases) when the starter is used to start a car (requiring very high current from the battery). This behavior is also true of other physical sources of power, such as generators, plasmas, ion beams, etc.

Since the *maximum* power that can be delivered by any physical source of electrical energy is *fixed and finite*, it can be seen from the expression **P = I*V** that the current *which the source can supply decreases* when the current is delivered at a higher voltage.

Consequently, charging sources, such plasmas, ion beams, etc., which induce high wafer surface potentials at some locations on the wafer may be less damaging (or even non-damaging) at those locations, because they may not be able to deliver sufficient current to cause damage.

Conversely, charging sources are often able to deliver *larger currents* at locations exhibiting lower potentials. If the potentials exceed the breakdown voltage of the oxide, greater damage will occur at these locations, even though the potentials are lower than at other locations on the wafer. This is illustrated in the resist ashing example included at the end of this tutorial. This behavior has been observed frequently – the example is not an isolated case.

What the J-V Plots Show

The CHARM-2 J-V plots are an empirical characterization of the ***current density vs. voltage characteristics of the charging source***, such as a plasma or ion beam, measured at each die location on the CHARM-2 wafer ***in the actual process environment experienced by the product wafers***.

The J-V plots show the net current density, J, in Amps/cm^2, that the charging source is capable of supplying, for all values of surface-to-substrate potentials. Having this information allows us to ***predict*** the likelihood of gate oxide damage for ***any*** oxide thickness. We are able to do this by using the J-V plots of the charging source and the Fowler-Nordheim characteristics for the oxide in question.

Determining the Probability of Gate Oxide Damage

To determine if charging damage to gate oxide is possible and likely in a process tool, two questions need to be answered:

a) Are the wafer surface-to-substrate **potentials** sufficiently high to force current into the gate oxide (i.e.. do the surface-to-substrate voltages approach the oxide breakdown voltage?), and
b) Are the gate oxide **currents** sufficiently high to cause damage during the time that the wafer is exposed to the charging currents?

Using the data from the CHARM-2 wafers, the WCM ChargeMap analysis software produces, among other formats, *wafer maps* of the surface-to-substrate potentials and *J-V plots,* with a spatial resolution of 8mm across the entire wafer. A simple visual inspection of the potentials wafer maps shows whether the surface-to-substrate potentials reached the oxide breakdown voltage. (If the gate oxides have not been characterized and the oxide breakdown voltage is not known, useful information can be obtained from the theoretical Fowler-Nordheim expression described later.)

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However, to determine if the gate oxide currents are sufficiently high to cause damage, we need to work with the CHARM-2 J-V plots of the charging source, and the gate oxide Fowler-Nordheim plots.

The Fowler-Nordheim (F-N) plot represents the gate oxide current-density vs. voltage characteristic, which can be obtained by applying different values of voltage across the gate oxide, and measuring the current which flows through the gate oxide. Dividing the current by the gate oxide area, yields the gate oxide current-density. The F-N plot is characteristic of the oxide for a given process. If this characteristic is not available, the theoretical F-N expression yields acceptable results. This expression is given by

$$J_{F\text{-}N} = \alpha\,(V_{ox}/t_{ox})^2\, e^{-(\beta t_{ox}/V_{ox})}$$

where $J_{F\text{-}N}$ is the gate oxide current density in A/cm^2, V_{ox} is voltage applied across the gate oxide, t_{ox} is the oxide thickness in cm, $\alpha = 1.88 \cdot 10^{-6}$ A/V^2, and $\beta = 2.55 \cdot 10^{8}$ V/cm.

To determine the gate oxide current density responsible for damage, we observe that the current which flows through the gate oxide is the net current density, J, collected by the "antenna", multiplied by the "antenna ratio", A_r, i. e., $J_{ox} = J * A_r$. [The "antenna ratio" is defined as A_r = (antenna area)/(gate oxide area)]. Since this current flows through the gate oxide, the charging source must deliver this current at nearly the oxide breakdown voltage. (To be exact, at a voltage which also satisfies the gate oxide Fowler-Nordheim plot.)

This suggests a simple graphical procedure to determine the value of J_{ox} . If the J axis of the CHARM-2 J-V plot is multiplied by the antenna ratio, Ar, and the gate oxide Fowler-Nordheim curve is superimposed on this graph, the intersection of the two curves is the value of J_{ox}.

The rationale for this procedure may also be stated as follows: The "antenna ratio"-multiplied J-V plot represents the values of the current density that the charging source can ***deliver*** to the gate oxide, at any value of gate-to-substrate potential. The Fowler-Nordheim (F-N) plot represents the values of the current density that the oxide can ***absorb***, at any value of gate-to-substrate potential. When gate oxide is being damaged, the current density absorbed by the gate oxide equals the current density delivered by the source. This value of current density, Jox, occurs at the intersection of the "antenna ratio"-multiplied J-V plot, and the gate oxide F-N plot.

If the two plots do not intersect [as shown in Figure 2 (a)], damage is not possible because the charging source, (e.g. plasma) is not delivering any current at the oxide conduction voltage. (i. e., J_{ox} = 0 at the gate oxide conduction voltage). The potential across the gate oxide will reach the maximum voltage measured at J = 0, but this will not cause gate oxide damage, just as charging and discharging storage capacitors in DRAMs causes no damage to capacitor gate oxides. If the two curves do intersect [as shown in Figure 2 (b)], damage is possible, and likely, because the charging source, (e.g. plasma) is delivering current at the oxide conduction voltage.

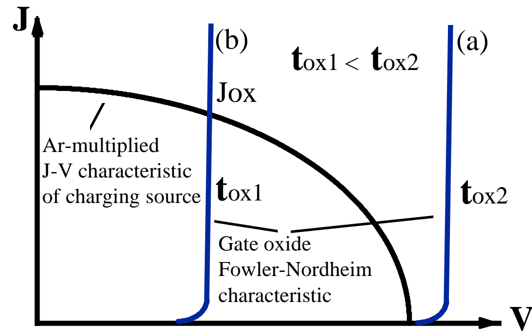

Figure 2. Oxide damage prediction: **(a)** FN plot does not intersect Ar-multiplied JV plot: damage is not possible; **(b)** FN plot intersects Ar-multiplied JV plot: damage is likely.

As previously mentioned, the extent of damage will depend on the magnitude of the oxide conduction current, J_{ox}, and the length of time, t_d, during which J_{ox} flows through the gate oxide. If $Q_{ox} = J_{ox} * t_d$ approaches Q_{bd}, serious damage to the gate oxide will occur. Onset of oxide damage has been observed when Q_{ox} reaches 0.1% to 1% of Q_{bd} **[1]**.

The time t_d is usually a small fraction of the total process time. During high current ion implants, t_d is on the order of 0.1 second to 1 second, while in plasma processes it is on the order of 10 seconds. Since the accumulated damage occurs in a rather short time, the values of J_{ox} responsible for the damage are reasonably large. Consequently, if the oxide F-N curves are not available, acceptable results will be obtained if, in the above analysis, the F-N plots are replaced by vertical lines at the gate oxide breakdown voltage.

It should be recognized that device structure effects, such as electric field enhancement along gate edges, the presence of n-wells and depletion regions, and the presence of photoresist may modify the J-V characteristics, or their impact on devices. We will discuss these topics in future issues of this bulletin.

Eliminating Gate Oxide Damage

It becomes apparent from the above analysis that gate oxides can be protected from damage by moving the charging source J-V characteristics to sufficiently low voltages, so the Ar-multiplied J-V plots do not intersect the gate oxide F-N characteristic. This is done by adjusting equipment operating parameters.

CHARM-2 wafers have been used to characterize the J-V characteristics of ion implanters, resist ashers, polysilicon etchers, oxide etchers, metal etchers, sputter processes, oxide depositions, metal depositions, as well as other processes where wafer charging was suspected. In future issues, we will describe our customers' successful, cost-effective, applications of CHARM-2 to yield improvement in these processes.

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CHARGING DAMAGE IN RESIST ASHER

To demonstrate the above principles, and especially to illustrate that regions of highest surface-to-substrate potentials *are not necessarily* the regions of greatest charging damage, we use an example of charging damage to 70A gate oxides in a resist asher.

Although the damage to antenna capacitors occurred in the center of the wafer **[2]**, the highest potentials measured with a CHARM-2 wafer occurred around the periphery of the wafer, as shown in **Figure 3a.** The potentials in the center of the wafer, shown in **Figure 3b,** were significantly lower.

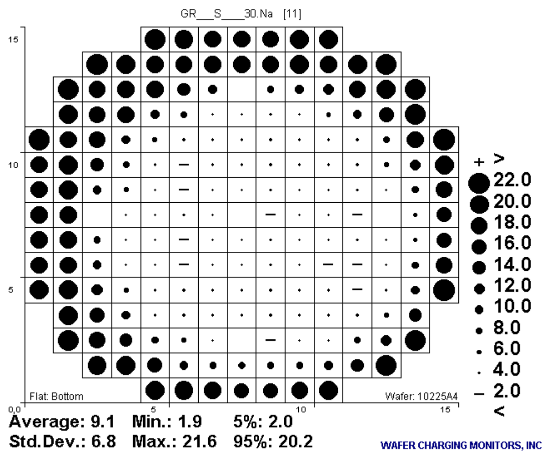

Figure 3a. Positive potentials recorded in a resist asher. (ChargeMap generates color wafer maps, as well.)

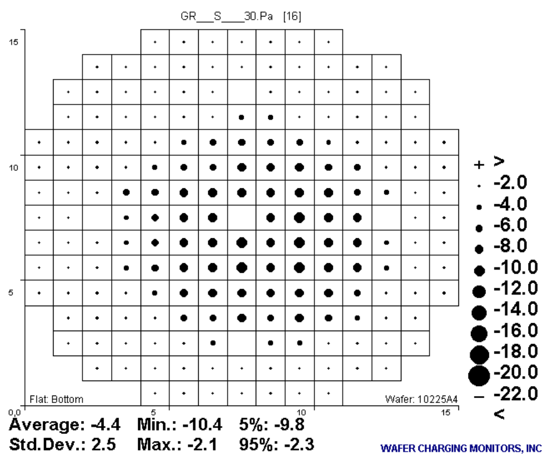

Figure 3b. Negative potentials recorded in a resist asher. (ChargeMap generates color wafer maps, as well.)

To understand why damage occurred in the center of the wafer, it is necessary to compare the positive and negative J-V characteristics of this charging source, shown in **Figure 3c.** **Figure 3c** shows that the negative current density, recorded in the center of the wafer, was significantly higher than the positive current density, recorded around the periphery of the wafer. As explained in the preceding tutorial, the damage thus occurred in the region of the highest current density**,** *not* in the region of the highest surface-to-substrate potential.

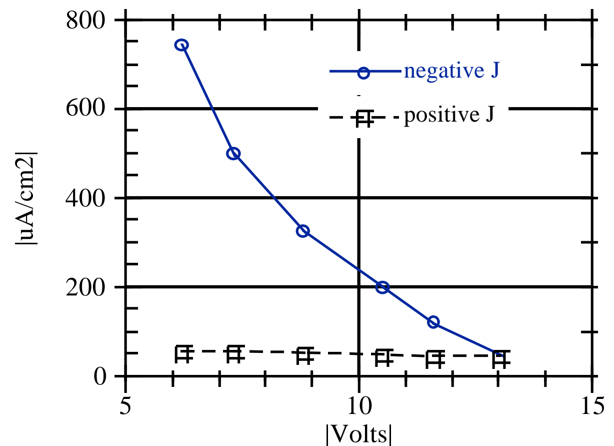

Figure 3c. Positive and negative current densities recorded in a resist asher. Positive JV come from die around the periphery of the wafer. Negative JV come from die in the center of the wafer.

References

[1] W. L. AbdelAti, S. Ma, T. C. Yang, J. P. McVittie, and K. C. Saraswat, "Measurement Strategy for Plasma Charging Induced Damage", Electrochemical Society Proceedings, PV955, 1995, pp. 410417.

[2] S. Fang, S. Murakawa, and J. P. McVittie, " Modeling of Oxide Breakdown from Gate Charging During Resist Ashing", IEEE Trans. on Electron Devices, Vol. 41, No. 10, October 1994, pp. 18481855.

FUTURE TOPICS:

In future issues we will present case studies of CHARM-2 applications and discuss CHARM-2 application procedures. We will discuss why device structure can increase or decrease device susceptibility to damage, and show the effect of resist placement and patterning on wafer charging – since it can play a dominant role during high current ion implants and etch processes. We will present summaries of informative publications and discuss frequently asked questions. We want this bulletin to become a forum for discussion of topics which can help you reduce charging damage to your products. If you have topics you'd like to learn about, or would like to contribute material to this bulletin, please contact us.

HOW TO CONTACT WCM:

If you are not on our mailing list, and would like to receive this bulletin or information about our products, services, and publications, please contact:

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