Wafer Charging Bulletin Vol. 2, No. 2

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From the Editor ...

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New and exciting ...

- **CHARM-2 measures potentials of one volt!**

Recent tests show that the new-generation 200 mm CHARM-2 wafers, when used in conjunction with on-site testing capability, are capable of measuring charging potentials as low as 1 volt in plasma processes, and about 1.5 volts in typical ion implant processes.

- **CHARM-2 detects transients.**

The accurate data conversion procedures implemented in WCM's ChargeMap® software permit CHARM-2 to distinguish between charging transients and steady-state charging, and to estimate the maximum duration of the charging transients. This additional capability allows more accurate assessment and diagnoses of equipment charging problems.

Relating CHARM-2 results to implant and plasma damage …

One of the most frequently asked questions about CHARM-2 is how to relate the CHARM-2 results to device damage. The answer to this question is the topic of this tutorial.

As a working example, we will use results obtained in a high-current, low energy ion implanter equipped with a plasma charge-control system. The conclusions will then be extended to plasma processes. We will compare CHARM-2 data to device damage results obtained on SPIDER-MEM transistors[1] with 4.5nm gate oxides implanted concurrently with the CHARM-2 wafers at three different settings of the plasma charge control system [1]. Antenna capacitors data will also be used to verify the conclusions.

Forget history !

In spite of historical concerns about positive charging in high-current ion implanters, and the moderately high positive potentials *and high current densities* observed on some splits in this experiment, no correlation was observed between SPIDER-MEM n-channel transistors V_t shifts[2] and CHARM-2 positive potentials, as shown in Figure 1. In particular, since the 4.5 nm oxide could not be damaged by potentials below 3 V, positive charging was clearly not responsible for the observed damage.

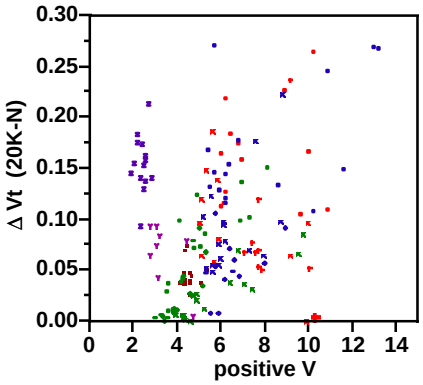

Figure 1. ΔVt on n-channel SPIDER-MEM transistors with 20K antenna ratios vs. positive potentials.

Although negative potentials were well above the breakdown voltage of the 4.5nm gate oxide, no correlation between transistor Vt shifts and negative potentials was observed either, as shown in Figure 2.

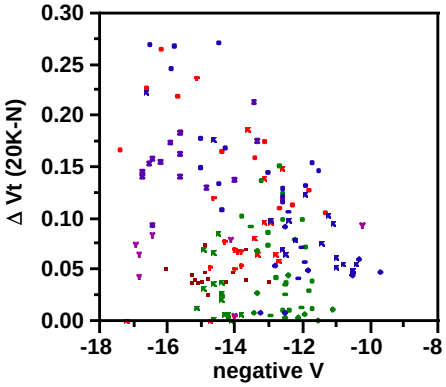

Figure 2. ΔVt on n-channel SPIDER-MEM transistors with 20K antenna ratios vs. negative potentials.

However, the negative potentials were sufficiently high to inject charge into the gate oxide. Consequently, very good

[1] The correlations between SPIDER-MEM data and CHARM-2 data were done on a site-by-site basis, i. e., both data came from the same (or nearest) location on the wafer.

[2] Ref. [1] also contains a discussion of p-channel results.

correlations were obtained between transistor parameter shifts and negative current densities at – 5 V (which is the estimated gate oxide voltage needed to cause current flow in the 45 Å gate oxide at the measured negative current densities). The scatter plot of V_t shifts of the n-channel transistor with 20K antenna ratio vs. negative current density at – 5 V is shown in Figure 3. The V_t shifts are positive, indicating trapped negative charge, which is expected for n-channel transistors under negative gate bias. The entire set of data for 8K, 20K, and 90K antenna ratios is shown in Figure 4.

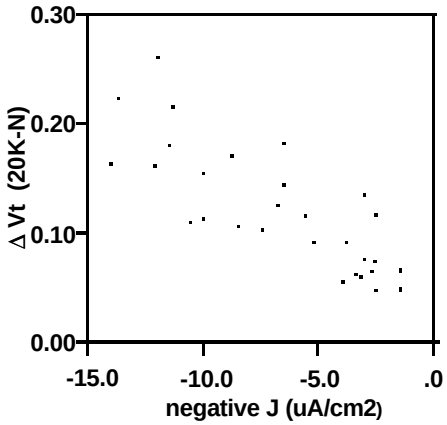

Figure 3. Site-by-site correlation between ΔV_t of n-channel transistors with 20K antenna ratio vs. negative current density at – 5 V.

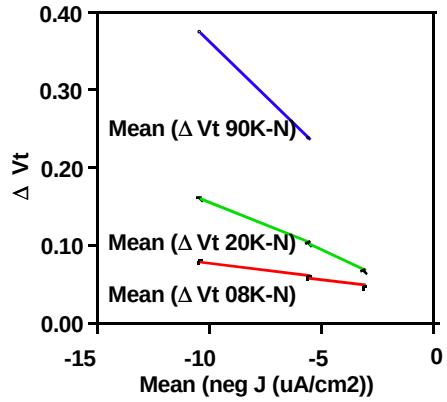

Figure 4. ΔV_t for n-channel transistors with 8K, 20K, and 90K antenna ratio vs. negative current density at – 5 V.

These results can be understood by taking into account the response of the SPIDER-MEM devices to the *pulsed* charging currents experienced in high current ion implanters[3]. The absence of correlation between damage to n-channel transistors and positive charging can be explained by depletion of the substrate under the gate and by the reverse-bias of the source/drain junctions, which absorb most of the applied voltage and thus significantly lower the voltage across the gate oxide, as illustrated in Figure 5. (Since the capacitance of the substrate is higher than device capacitances, the substrate potential lags the gate and source/drain potentials, giving rise to the depletion regions illustrated in Figure 5.)

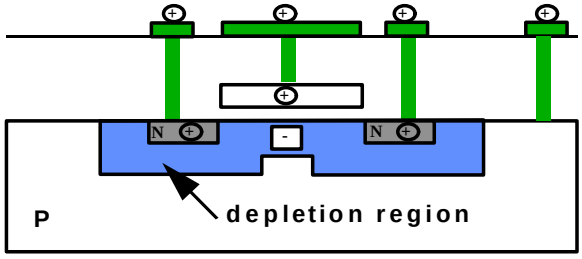

Figure 5. Response of n-channel SPIDER-MEM transistor to positive charging. The depletion region around source/drain junctions and under the gate protects the gate oxide from damaging potentials.

Consequently, when exposed to positive charging, the response of the SPIDER-MEM n-channel transistors is such that the voltage across the gate oxide is reduced to levels which do not cause charge injection into the oxide. No damage is caused in that case, hence V_t shifts are not correlated to positive charging parameters.

Negative charging, on the other hand, accumulates the p-substrate of the n-channel transistors, exposing the gate oxide to the entire gate-substrate potential. Since the negative gate-substrate potentials are sufficiently high to cause electron injection into the gate oxide, the V_t shifts are positive, and proportional to the magnitude of the negative current density, as shown in Figures 3 and 4.

The damage to SPIDER-MEM p-channel transistors also did not correlate to positive or negative potentials, but correlated to negative current densities. Since the analysis is more complicated, and the SPIDER-MEM p-channel results do not apply to product wafers, we refer the interested reader to reference [1] for the details[4].

The above analysis may be extended to anticipate correlations between CHARM-2 results and damage to device structures during different processes. In general, we need to consider what happens to n and p-channel device structures under positive and negative charging conditions.

Product ion implantation …

During product source/drain implants, device structures are simpler than the SPIDER-MEM transistors[5] and are easier to analyze.

N-channel devices, consisting of gate electrodes over p-substrate, are very susceptible to negative charging. Negative charge on the gate causes accumulation of the p-substrate, and the entire surface-substrate potential appears across the gate oxide. Consequently, damage will be proportional to the magnitude of the negative current density injected into the gate oxide. We thus expect to observe correlations between device damage (ΔVt, ΔGm, 1/f noise, etc.) and negative current density measured at the oxide conduction voltage[6].

[3] In high current ion implanters wafers spin past the beam, resulting in device exposure to positive and negative charging transients of ~ 1 ms duration [2].

[4] This paper is also available from the WCM web-site.
[5] No source/drain, well, or substrate probe pads are present.
[6] Refer to WCM Bulletin vol.1 no.1 for a discussion of this topic.

Conversely, n-channel devices are considerably less susceptible to positive charging. Pulsed positive charge on the gate causes deep-depletion of the p-substrate, and most of the surface-substrate potential is dropped in the substrate. Since only a small fraction of the surface-substrate potential appears across the gate oxide, it is typically insufficient to cause charge injection into the oxide. In that case, positive charging does not damage the n-channel device. Excessive positive charging may still cause device damage, however, such conditions are infrequent in properly functioning, present generation ion implanters. Consequently, we would not expect correlations between device damage and positive potentials or positive current densities[7], unless serious equipment problems are present. (Exceptions to this could occur in older equipment. Flood system upgrade will likely cure this.)

Besides the SPIDER-MEM example discussed previously, these conclusions are supported by data obtained on antenna capacitors built on p-substrates[8], as shown in Figure 6. This data also illustrates how substrate type polarizes the response of the antenna capacitors. The failure rate of the antenna capacitors in Figure 6 increases with increasing plasma flood setting, which results in increasing negative charging. The lowest damage is obtained with the flood OFF, which results in lowest negative charging and highest positive charging. Clearly, antenna capacitors built on p-substrate are sensitive to negative charging, but not to positive charging. Conversely, antenna capacitors built on n-substrate are sensitive to positive charging, but not to negative charging.

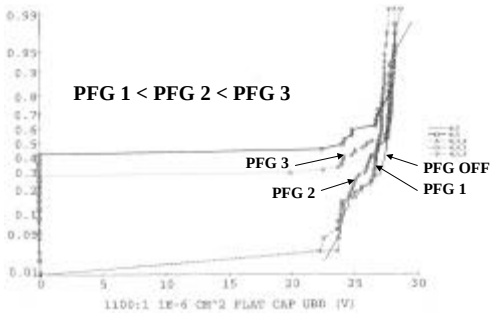

Figure 6. Antenna capacitors breakdown voltage vs. plasma flood setting (p-substrate; antenna ratio = 1100:1; PFG 3 = high setting; PFG 1 = low setting).

It is very important to recognize this difference in response when selecting or developing a monitor for a given application. For example, in contemporary CMOS (built on p-substrate), n-substrate antenna capacitors are not a good choice for implant monitors since damage to devices built in p-substrates will most likely result from negative charging, while n-substrate antenna capacitors are sensitive to positive charging.

P-channel devices, consisting of gate electrodes over n-wells in p-substrate, are less susceptible to charging damage during ion implantation than N-channel devices. Pulsed negative potential applied to the gate of p-channel device causes deep depletion of the local substrate (n-well). Consequently, most of the surface-substrate potential is dropped in the n-well. Since only a small fraction of the surface-substrate potential appears across the gate oxide, the probability of damage is greatly reduced. Consequently, we would not expect correlations between device damage and negative current densities, unless serious equipment problems are present.

P-channel devices, on the other hand, are somewhat more susceptible to positive charging. Pulsed positive charge on the gate of p-channel device causes accumulation of the local substrate (n-well), and the entire surface-substrate potential initially appears across the gate oxide. If positive voltages are not suppressed by the charge control system, the gate oxide will conduct. If the n-well were absent, the high positive current densities would cause disastrous damage. However, as soon as the gate oxide begins to conduct, the positive current injected into the n-well reverse-biases the n-well/substrate junction. This reduces the voltage across the gate oxide and turns down the oxide current, thereby limiting the damage. However, because this event occurs each time the p-channel device passes under the beam, some damage is expected if positive potentials are not adequately suppressed. Because the amount of charge required to reverse-bias the n-well/substrate junction depends on the magnitude of reverse bias, damage in this case will correlate with the magnitude of positive potentials, but will be independent of the magnitude of positive current density. However, because the amount of charge required to reverse-bias the n-well/substrate junction is proportional to the size of the junction, the magnitude of the damage will also increase with the size of the n-well.

In summary, when the charging characteristics of present generation ion implanters are taken into account, we conclude that charging damage in p-substrate CMOS will most likely occur to n-channel devices as a result of excessive negative charging (over-flooding). (We assume that the equipment is operated according to manufacturers' recommendations, and is not malfunctioning.) Of course, the status of the equipment is easily verified with CHARM-2 wafers, and which may be compared to manufacturers' CHARM-2 data.

Plasma processes …

With regard to charging, plasma processes differ from ion implantation in two significant ways. Although RF driven, charging currents in plasma processes are typically steady-state currents, not repeated transients as in the case of ion implants. In addition, plasma processes are accompanied by high levels of UV emissions [3], which reduce the protective effects of depletion layers and reverse-biased junctions[9], and cause additional damage [4]. These two differences significantly modify the conclusions reached previously.

[7] Since positive charging in high current ion implanters is typically accompanied by high current densities (compared to negative charging), correlations to positive potentials could occur in cases where positive potentials are so high that substrate depletion effects are insufficient to protect the gate oxide.

[8] Data provided by David Hess of Philips Semiconductors.

[9] Many down-stream ashers do not expose wafers to UV emissions.

Regarding n-channel devices exposed to negative charging, the conclusions remain unchanged. However, n-channel devices exposed to positive charging are affected by UV. Since UV generates electron-hole pairs in the silicon substrate, under steady-state charging the deep-depletion layer collapses due to the formation of an inversion layer under the gate. This increases the voltage across the gate oxide, thereby significantly increasing the probability of damage from positive charging. This is particularly true of high-density plasmas, where very high UV intensity and very high positive charge fluxes are present. Consequently, in plasma equipment damage to n-channel devices can occur as a result of both negative and positive charging, and, therefore, can correlate to negative current density, positive current density, and UV intensity.

P-channel devices are affected by UV during both negative and positive charging. During negative charging, the deep-depletion region, which would form under the gate in the absence of UV, collapses in the presence of UV due to the formation of an inversion layer. This increases the voltage across the gate oxide, thereby significantly increasing the probability of damage from negative charging. In the case of positive charging, the protection offered by the reverse-biased n-well/substrate junction is disabled by junction leakage caused by UV. Consequently p-channel devices become more vulnerable to damage from negative and positive charging in the presence of UV. Damage might thus correlate to negative current density, positive current density, and UV intensity.

In summary, the presence of UV (and steady-state charging, which allow inversion layers [3] to form) in plasma processes disable the inherent protection mechanisms that depletion layers and reverse-biased junctions provide during ion implantation. In addition, UV allows oxides to conduct [3], thereby providing another mechanism for device damage. As a result of UV emissions and the higher current densities present in high density plasma equipment, HDP equipment is potentially much more damaging than high current ion implanters.

Although UV has a significant influence on the response of device structures to surface charging, its impact depends on the particular process. Since photoresist absorbs UV, contact and via etching processes will be less influenced by UV (since most of the wafer is covered by resist) than polysilicon etching, metal etching, and oxide deposition processes (where most of the wafer is exposed to UV).

Device structures evolve …

When attempting to relate wafer charging to device damage, we should also keep in mind that device structures change as wafers proceed through the process flow. Conclusions reached about charging during ion implantation or gate etching may not apply to contact or metal etching, since device structures in these processes allow charging currents to enter the n-wells and the substrate. This will change the bias of the n-wells and substrate, which may change the bias across the gate oxides, or forward-bias junctions which, due to minority carrier injection, may significantly affect the response of the device structure to the charging stimulus (as in the case of SPIDER-MEM p-channel devices under negative charging conditions [1]).

Conclusions

1. The variables used to correlate device damage to charging parameters, such as potentials and current densities, should be chosen carefully. The interaction between a charging source, the device, and the nature of the resultant damage, depend on the device structure and its device physics. Consequently, the correlation variables must be chosen on the basis of device physics of the given structure, as shown in this publication.

2. UV can have a significant influence on the *response* of device structures to the charging environment, due to UV-generated inversion layers and leaky junctions. Both lead to increased potentials across gate oxides, thereby increasing the probability of gate oxide damage. Moreover, UV allows oxides to conduct, thereby providing another mechanism for device damage. The role of UV in charging damage should not be overlooked, but it will be moderated by resist coverage.

3. Device structures change during the IC process flow. Conclusions that apply to device structures present during one process may not apply to device structures present during another process. Similarly, conclusions that apply to one test vehicle may not apply to another test vehicle. Each device structure, or test vehicle, should be considered on its own.

Please note that the above discussions did not consider how the charging stress was generated (e. g., plasma non-uniformity, topography-dependent charging, etc.). They only considered the response of device structures to the applied stress, regardless of its origin.

References

[1] W. Lukaszek, M. Rendon, and D. Dyer, P2ID99, pp. 200-203.
[2] B. J. Doherty and D. J. McCarron, NIMB, B37/38, p. 559, 1989.
[3] C. Cismaru, J. Shohet, and J. McVittie, P2ID99, pp. 192-195.
[4] S. Lin, B. Tsui, C. Tsai,and C. Hsia, P2ID99, pp. 41-44.

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CHARM applications. If you have topics you'd like to learn about, or would like to contribute material to this bulletin, please contact us.

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