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Device Effects and Charging Damage: Correlations Between SPIDER-MEM and CHARM®-2

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Abstract

The reasons underlying correlations and lack of corrrelations between SPIDER-MEM and CHARM-2 results are investigated for wafers inplanted in a high-current, low energy ion implanter equipped with a plasma charge-control system. The results can be explained by taking into account the device structure and physics of the SPIDER-MEM devices, and the charging characteristics of the implanter. The work has important implications for comparisons of results obtained from charging monitors and damage monitors.

I. Introduction

Charging damage to ICs can result in costly losses of product. In order to provide rapid feedback for process control and process optimization, monitors such as SPORT [1], CHARM-2 [2], and the SPM [3] technique have been developed to provide measurement of plasma parameters associated with charging damage, such as wafer surface potentials, J-V characteristics of the plasma at the wafer surface, and UV intensity. Whether these monitors are considered useful or not is typically judged by observing correlations (or lack of correlations) to product yield or shifts in transistor parameters. However, it may not be obvious which variables should be used to look for correlations. For example, should yield or device parameters correlate to potentials, current densities, or UV intensity? Which plasma parameters should correlate with damage to n-channel transistors, and which should correlate with damage to p-channel transistors? Which transistor parameters should be used to look for correlations: V_t shifts, G_m shifts, gate leakage current, or others? A wrong choice of variables could lead to lack of correlation and the elimination of a potentially useful technique, or important information could be missed resulting in, or prolonging, undesired situations.

This paper presents some answers to these and related questions learned from a detailed examination of data obtained with Sematech SPIDER-MEM and CHARM-2 used concurrently in experiments performed on a new generation ion implanter equipped with a plasma charge control system. Excellent correlations were observed between some SPIDER and CHARM-2 variables, while no correlations were observed between other variables. An investigation of these observations showed that the explanations lie in the device physics of the SPIDER-MEM structures, and their interaction with the charging source. Our approach can be generalized to other charge monitoring techniques used in any plasma-based processing tool.

I. Description of experiment

The data analyzed here was obtained from three bare SPIDER-MEM wafers and three bare CHARM-2 wafers implanted concurrently with Arsenic in a high current, low energy ion implanter at three different settings of the plasma charge control system.

The SPIDER-MEM data came from n-channel and p-channel transistors with 45 Å oxides. The transistor gate electrodes were connected to charge collecting antennas on the surface of the wafers. The antenna ratios were 8K, 20K, and 90K. Transistor V_t, G_m, and gate leakage current at 2.5 V were measured before and after the experiment to determine changes in these parameters due to wafer charging.

The CHARM-2 data included wafer maps of positive and negative surface-substrate potentials, and positive and negative J-V characteristics of the charging sources.

The correlations between SPIDER-MEM data and CHARM-2 data was done on a site-by-site basis, i. e., both data came from the same (or nearest) location on the wafer.

III. Experimental results

Significant non-uniformities in positive and negative charging were recorded with the CHARM-2 wafers at all settings of the plasma charge control system. This was fortuitous, since it allowed correlations over a relatively large range of charging parameters using only three charge control system settings. Typical positive and negative J-V plots recorded in a column of die across the wafer are shown in Figures 1 and 2. It can be seen that both positive and negative charging sources are neither voltage sources, nor current sources, but voltage dependent current sources, i. e., the magnitude of the

current density depends on the value of the surface-substrate potential[1].

Due to historical concerns about positive charging in high-current ion implanters, and the high positive potentials and current densities observed in this experiment, the first correlations performed were between SPIDER-MEM transistors V_t shifts, G_m shifts, and CHARM-2 positive potentials. A coincidental inclusion of data from another experiment which showed positive potentials well below the breakdown voltage of the SPIDER gate oxides, but very high transistor parameter shifts, made it clear that positive charging was not responsible for the observed damage.

Correlations to negative potentials, which were relatively uniform over the wafers, were also absent, as shown in Figure 3 for n-channel transistors. Similar results were obtained for p-channel transistors. This is not surprising, since charging damage is due to current flow through oxides, and potentials are measured at J = 0.

However, very good correlations were obtained between transistor parameter shifts and negative current densities at – 5 V (which is the estimated gate oxide voltage needed to cause current flow in the 45 Å gate oxide at the measured negative current densities)[2]. The scatter plot for the V_t shift of the n-channel transistor with the 20K antenna ratio vs. the negative current density at – 5 V is shown in Figure 4. The V_t shift is positive, indicating trapped negative charge, which is expected for n-channel transistors under gate injection conditions. The entire set of data for the 8K, 20K, and 90K antenna ratios is shown in Figure 5. The antenna effects are evident, as is saturation of V_t shift at the largest antenna ratio.

The corresponding results for the p-channel transistors are shown in Figure 6. Although the trends are similar as for the n-channel transistors, the V_t shift is negative, indicating positive charge trapping. A threshold current for the onset of damage is also evident.

IV. Analysis of results

The results presented in section III can be explained by taking into account the response of the SPIDER-MEM devices to the *pulsed* charging experienced in a high current ion implanter[3]. In particular, since both positive and negative charging sources are current sources, the potentials on different nodes depend on the capacitances associated with those nodes, giving rise to voltage differences across oxides or junctions even when the gate, junction, and substrate probe pads are exposed to the same charging source.

The absence of correlation between damage to n-channel transistors and positive charging can be explained by depletion of the substrate under the gate and by the reverse-bias across the source/drain junctions, which significantly lower the voltage across the gate oxide, as illustrated in Figure 7. (Since the capacitance of the substrate is higher than device capacitances, the substrate potential lags the gate and source/drain potentials, giving rise to the depletion regions illustrated in Figure 7.)

The absence of correlation between damage to p-channel transistors and positive charging, on the other hand, can be explained by reverse bias of the n-well-substrate junction which ensures that the n-well potential closely follows the gate potential, as illustrated in Figure 8.

Consequently, under positive charging conditions, the response of the SPIDER-MEM devices is such that it reduces the voltage across the gate oxide to levels which do not cause charge injection into the oxide. No damage is caused in that case, hence, $\mathbf{V_t}$ and $\mathbf{G_m}$ shifts are not correlated to positive charging parameters.

Negative charging, on the other hand, results in a different response. The substrate of the n-channel transistors is accumulated, exposing the gate oxide to the entire gate-substrate potential. As evident from Figure 2, the gate-substrate potentials are sufficiently high to cause electron injection into the gate oxide. Consequently, the $\mathbf{V_t}$ shifts are positive, and proportional to the magnitude of the negative current density, as shown in Figures 4 and 5.

The response of the p-channel transistor to negative charging is more complex, because it has to account for positive charge trapping resulting from the application of negative currents. As can be seen from Figure 9, positive charges can be injected into the gate oxide during that portion of the charging transient when the well-substrate junction is forward-biased and injects minority carriers (holes) into the well [5]. If the well-substrate capacitance is larger than the source/drain or gate capacitance, the latter will be negatively biased relative to the n-well, creating depletion regions around the source/drain junctions and under the gate, similar to the n-channel transistor under positive bias. The injected holes will be accelerated by the electric field in the depletion region under the gate, and injected into the gate oxide, causing positive charge trapping and negative $\mathbf{V_t}$ shifts. In this case, the threshold current density for the onset of damage, evident in Figure 6, is the current density needed to reach forward bias of the well-substrate junction during the brief duration of the charging transient. One of the

[1] In high-current ion implanters, both positive and negative charging is observed at the same location on the wafer. However, the positive and negative charging events occur at different times [4].

[2] In essence, this is the estimated gate oxide voltage at the intersection of the gate oxide F-N plot with the negative J-V plots shown in Figure 2 [2].

[3] In high current ion implanters, the wafers spin past the beam, resulting in device exposure to positive and negative charging transients of ~ 1 ms duration [4].

objectives of future work is to confirm this model by applying the CHARM-2 measured currents to the p-channel devices with the use of a tester, to verify the response.

V. Transistor parameter shifts vs. gate leakage

Due to the popular use of oxide leakage current as indicator of oxide damage, the change in gate leakage current of n and p-channel transistors was also measured. The scatter plot of ΔI_g vs. ΔV_t for n-channel transistor with 20K antenna is shown in Figure 10. Similar results were obtained for other devices. Although the lack of correlation between ΔI_g and ΔV_t may seem surprising, it is reasonable to suggest that different mechanisms are responsible for ΔV_t and ΔI_g. ΔV_t is due to trapped charge over the entire gate area, whereas I_g could be associated with localized imperfections in the gate oxide.

VI. Conclusions

Several conclusions may be drawn from this experiment.

1. The variables used to correlate device damage to charging parameters, such as potentials and current densities, should be chosen carefully. The interaction between a charging source, the device, and the nature of the resultant damage, depends on the device structure and its device physics. Consequently, different damage monitors may respond differently to the same charging source, or apparent lack of correlation between a charging monitor and a damage monitor may be due to an inappropriate choice of variables. The correlation variables should be chosen on the basis of device physics of the structure in question.

2. Wafer surface potentials may not correlate to device damage. Whether they do, or do not, depends on the J-V characteristics of the charging source.

3. Oxide leakage current is a "noisy" monitor, and is not optimal for process optimization work.

VII. Acknowledgements

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VIII. References

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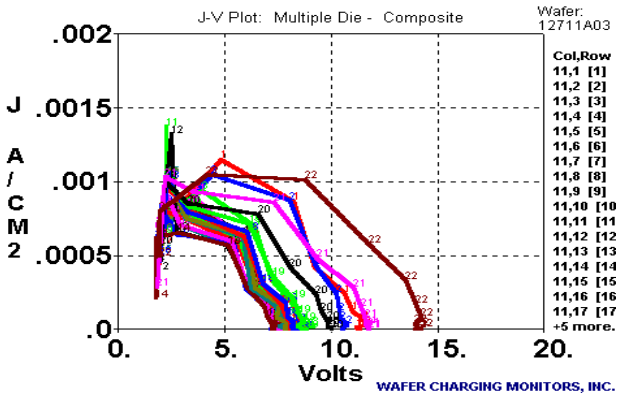

Figure 1. Typical positive J-V plots obtained in a column of die across the wafer. The asymptote at ~ 2 V is an artifact of the data conversion procedure and should be ignored.

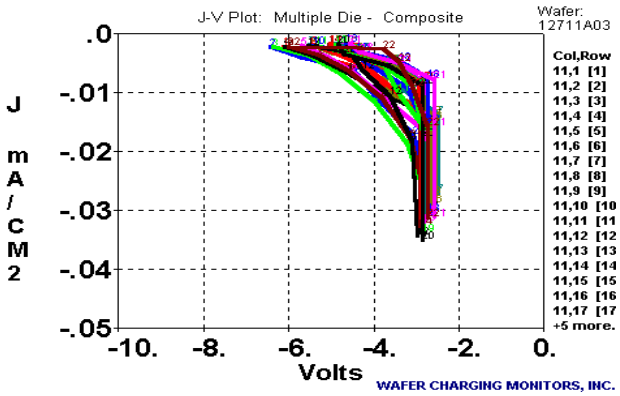

Figure 2. Typical negative J-V plots obtained in a column of die across the wafer. (Note change in J scale.) The asymptotes at ~ - 2.5 to 3 V are an artifact of the data conversion procedure and should be ignored.

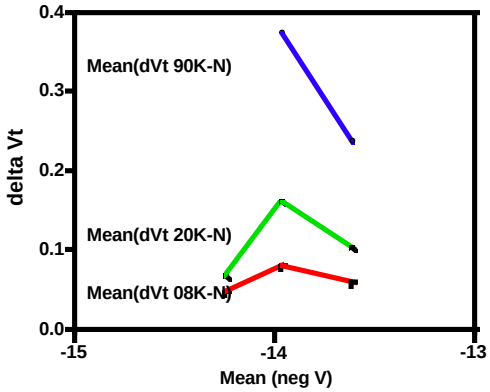

Figure 3. Average ΔV_t vs. average negative potential for 8K, 20K, and 90K antenna ratios n-channel transistors. (No correlation.)

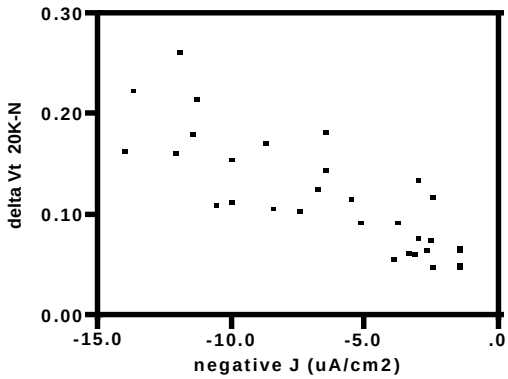

Figure 4. Site-by-site correlation between the V_t shift of the n-channel transistor with the 20K antenna ratio vs. negative current density at – 5 V.

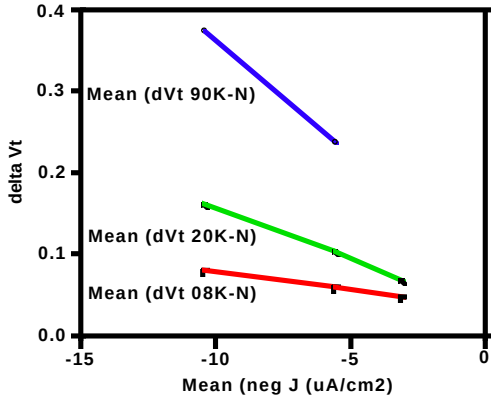

Figure 5. V_t shift for n-channel transistors with 8K, 20K, and 90K antenna ratio vs. negative current density at – 5 V.

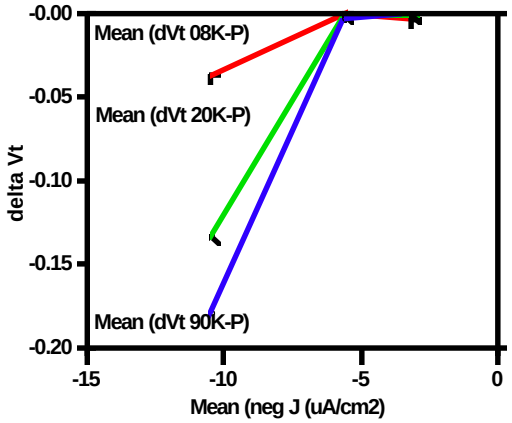

Figure 6. V_t shift for p-channel transistors with 8K, 20K, and 90K antenna ratio vs. negative current density at – 5 V.

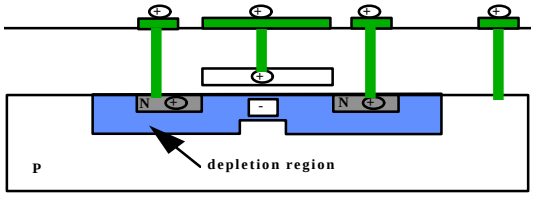

Figure 7. Response of n-channel SPIDER-MEM transistor to positive charging. The depletion region around source/drain junctions and under the gate protects the gate oxide from damaging potentials.

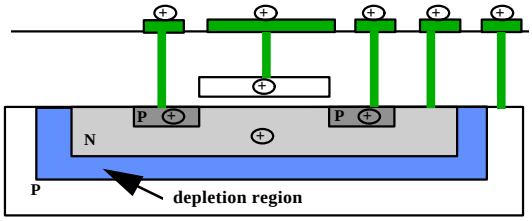

Figure 8. Response of p-channel SPIDER-MEM transistor to positive charging. The reverse-bias across the well-substrate junction keeps the well at nearly the same potential as the gate, thus protecting the gate oxide from damaging potentials.

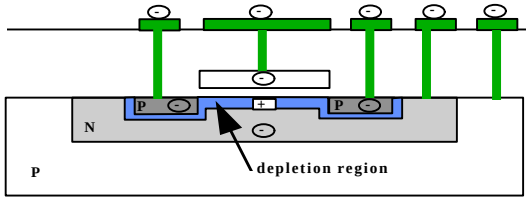

Figure 9. Response of p-channel SPIDER-MEM transistor to negative charging. The well-substrate junction is forward-biased and injects holes into the n-well. The holes are accelerated in the depletion region under the gate, and injected into the oxide.

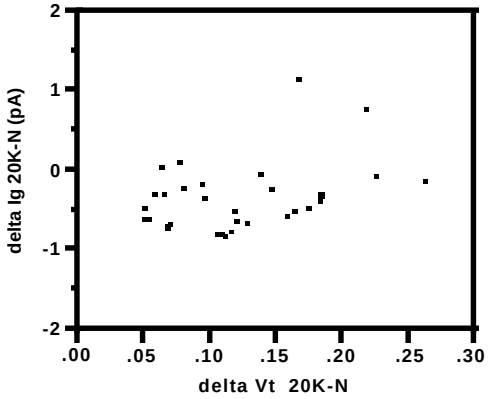

Figure 10. Lack of correlation between ΔI_g and ΔV_t.