WAFER CHARGING MONITORS, INC.

USING CHARM®-2 TO QUANTIFY WAFER CHARGING IN ION AND PLASMA-BASED IC PROCESSING EQUIPMENT

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This introduction to CHARM-2 charging monitors is intended to briefly explain the basics of CHARM-2 wafers, and to illustrate some applications possible with the use of CHARM-2 charging monitors.

This presentation is **not** a complete survey of all possible applications. If you have questions about applications not included here, please contact Wafer Charging Monitors. It is very likely that we have experience with them, as well.

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Contents ...

- **About CHARM®-2**
- **Brief description of CHARM®-2 monitors**
- **Damage prediction using J-V plots**
- **Ion implant product damage**
- **Wafer charging in ion implanters**
  - electron flood effects
  - photoresist effects
- **Wafer charging in**
  - asher
  - polysilicon etcher
  - metal etcher
  - oxide etcher (resist effects)
  - oxide deposition
- **CHARM®-2 as equipment diagnostic**
- **List of CHARM®-2 applications**
- **WCM products and services**

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About CHARM®-2 ...

- **CHARM®-2 is a wafer charging monitor system for quantifying wafer charging in IC process equipment.**
- **The CHARM®-2 system provides:**
  - Wafer maps of surface-substrate potentials
  - J-V plots of charging currents
  - Wafer maps of UV dose
  - 8mm by 8mm spatial resolution
- **CHARM®-2 wafers are used to measure charging in:**

ion implanters	oxide etchers
resist ashers	sputter cleans
polysilicon etchers	oxide depositions
metal etchers	metal depositions

- **The CHARM®-2 system consists of:**
  - CHARM®-2 wafers (100, 125, 150, or 200 mm)
  - Keithley or HP CHARM®-2 test software (calibration, programming, and measurement)
  - WCM data conversion, analysis, and display software
- **Advantages of CHARM®-2:**
  - measures variables responsible for device damage
  - excellent correlation to device damage
  - CHARM®-2 wafers are **re-usable** ⇒ cost-effective
  - reproducible results (CHARM®-2 wafers are calibrated)
  - rapid turn-around (results in < 1 hour)
  - separation of charging effects from UV effects
  - no wires; no modification to equipment

CHARM-2 wafers are very easy to use. Just put them in the process chamber and run the process (or an abbreviated process). The CHARM-2 wafers are then tested on a parametrict tester to read out the stored data. Following this, they are re-programmed on a parametric tester to erase the stored data, and they are ready for the next application.

The parametric test data is processed with PC-based WCM ChargeMap data analysis software to obtain wafer maps of surface-to-substrate potentials, UV intensity, and J-V plots of the equipment charging characteristics.

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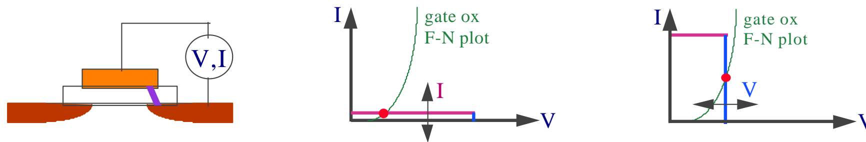
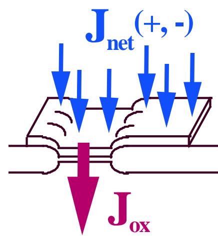
Fundamentals of charging damage ...

- **Device damage during electrical characterization ...**



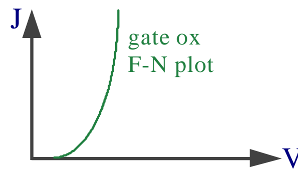
- **Device damage in IC process equipment ...**

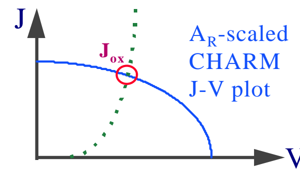


$J_{ox} = J_{F\text{-}N} = A_R\, J_{net}$
$Q_{ox} = J_{ox}\,(\text{time}) = A_R\, J_{net}\,(\text{time})$
if $Q_{ox} \rightarrow Q_{BD} \Rightarrow$ severe damage
onset of damage at 0.1 % - 1% of Q_{BD}

- **To understand (predict) damage, we need**

Gate ox F-N plot + **Equipment J-V plot**





Electrical damage to gate oxides has been studied for many years with electrical test techniques, where the oxides are exposed to current-sources or voltage-sources and the resultant changes in device characteristics (damage) are monitored. The damage is due to charge trapping in the oxide or at the oxide-silicon interface caused by Fowler-Nordheim current that flows through the oxide as a result of the application of the current-sources or voltage-sources connected to the gate electrode.

Process-induced damage in ion and plasma-based IC process equipment also occurs as a result of Fowler-Nordheim current flowing through the gate oxide. However, in this case the charging source is the net current density, Jnet, composed of ions and electrons collected by the gate electrode. This charging source is neither a current-source, nor a voltage-source, but a voltage-dependent current-source. Consequently, it is essential to know the J-V characteristics of the charging source to determine the oxide current, Jox, responsible for damage.

The oxide current, Jox, is determined from the intersection of the "antenna-ratio" scaled J-V plot, determined with a CHARM-2 wafer, and the oxide Fowler-Nordheim characteristics.

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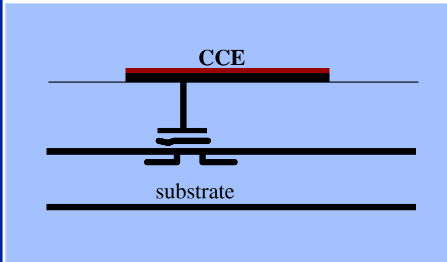
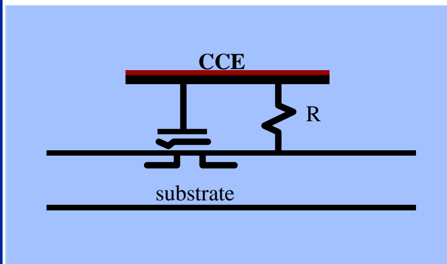
Each CHARM®-2 die contains:

• Volt-meters:



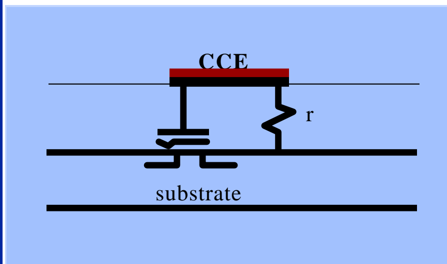
- Similar to “antenna capacitors”
- EEPROM senses and records CCE voltage
- More sensitive than “antenna” capacitors
- Calibrated to measure Volts (including polarity)

• Current-meters:



- Volt-meters with calibrated current-sensing resistors
- EEPROM records the voltage across the current-sensing resistor
- Calibrated to measure current density in Amps/cm^2 (including polarity)

• UV-meters:



- Small CCE and small “r” suppress charging effects
- Change in EEPROM threshold voltage is proportional to UV dose

Because CHARM-2 sensors are composed of circuit elements (EEPROM transistors, resistors, and diodes) whose behavior is well-understood and characterized, the response characteristics of the CHARM-2 sensors are fixed by design. Consequently, the interpretation of CHARM-2 results is unambiguous.

Because separate, individually optimized, sensors are used to measure electrostatic charging vs. UV, charging effects and UV effects are never confused. This is particularly important for plasma applications, where the UV intensity is usually very high.

A complete discussion of the principles of operation of the CHARM-2 sensors is contained in WCM Technical Note 1: "The Fundamentals of CHARM-2", available from Wafer Charging Monitors, Inc.

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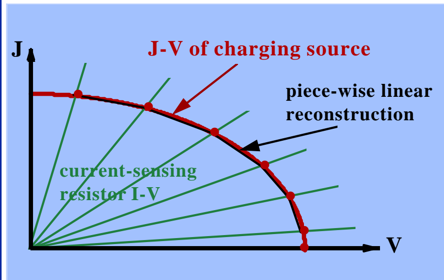
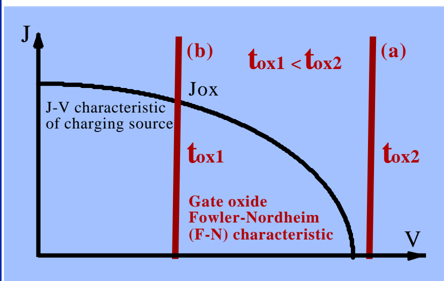
Predict damage with CHARM®-2:

- **Measure the J-V characteristics of the charging source with the CHARM®-2 passive plasma probe:**



- Implemented with multiple current-meters
- Each current-meter provides one point on the J-V plot
- CHARM-2 measures the J-V characteristics of charging source on the surface of the wafer using substrate as the voltage reference

- **Predict gate oxide damage with the J-V of the charging source and the gate oxide Fowler-Nordheim plot:**



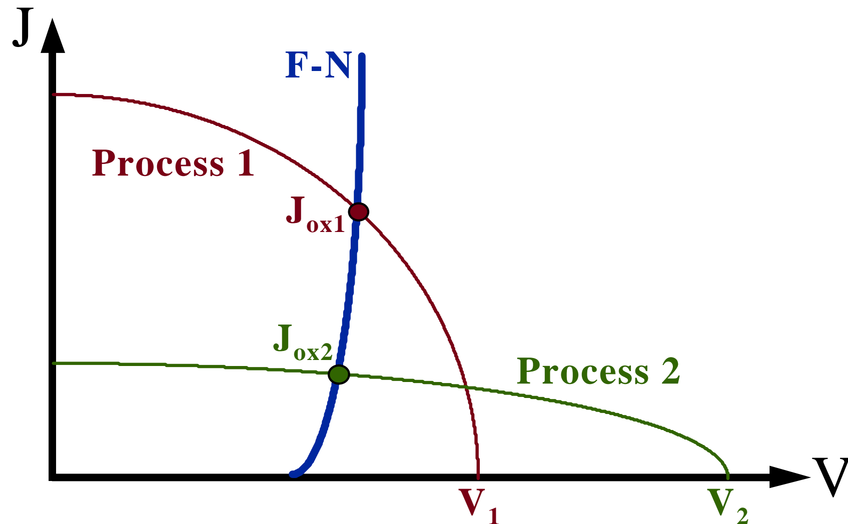
- (a) Damage not possible since F-N plot does not intersect J-V plot
- (b) Damage possible since F-N plot intersects J-V plot (charging source forces current into oxide)

The CHARM-2 passive plasma probe may also be thought of as on-wafer, wireless, Langmuir probe. The important difference between the two is the voltage reference: the Langmuir probe uses the wall of the process chamber, whereas CHARM-2 uses the wafer substrate. Since gate oxide damage is due to voltage difference between the surface of the wafer and the substrate, CHARM-2 J-V plots may be used to predict product damage, where as Langmuir probe plots may not.

Prediction of charging damage using CHARM-2 data is discussed in detail in WCM Technical Note 2: "Understanding CHARM-2 Data and its Relationship to Charging Damage", available from Wafer Charging Monitors, Inc.

Potentials can be misleading ...

- **Process 1 is more damaging than Process 2, even though wafer potentials would suggest the opposite.**



Although the wafer surface-substrate potential for Process 2 is larger than the wafer surface-substrate potential for Process 1 ($V_2 > V_1$), Process 1 is capable of forcing significantly larger current density into the gate oxide than Process 2 ($J_1 > J_2$). Consequently, Process 1 is significantly more damaging than Process 2.

It should be recognized that potential sensors (voltmeters) are very high input impedance instruments, which do not draw any current from the charging source whose voltage they measure (i. e., voltage is measured at J = 0). Consequently, a voltage measurement does not say anything about the amount of current a charging source can deliver. However, charging damage depends on the amount of charge that passes through the gate oxide, which depends on the current that passes through the oxide (Qox = Jox * tchg). Since the charging time, tchg, is similar for most processes, the quantity which determines the extent of damage is the oxide current density, Jox. Consequently, the charging source which can force the most current into the gate oxide (Jox1) will also do the most damage.

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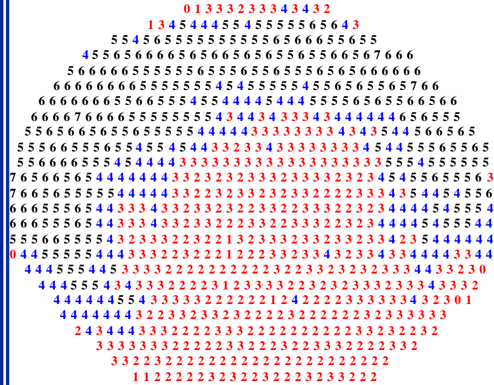
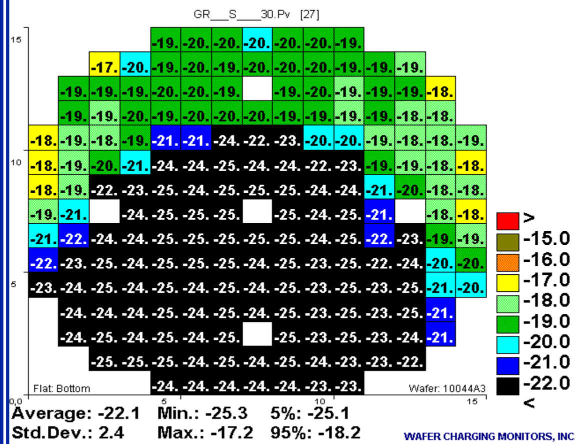
CHARM®-2 data correlates with product yield:

- **Product yield:**



- Composite yield map of 140 product wafers
- Low numbers indicate low yield

- **CHARM®-2 negative potentials :**



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- Region of high negative potentials (black) corresponds to region of reduced product yield

Ref.: J. Shideler, et. al., "A New Technique for Solving Wafer Charging Problems", Semiconductor International, Vol. 18, No. 8, July 1995, pp. 153-158.

This example shows the spatial correlation between region of reduced yield on 140 EEPROM product wafers and the region of very high negative voltages recorded with the CHARM-2 wafers. (CHARM-2 voltmeters are saturated - the actual values are higher than indicated in the CHARM-2 wafer map.) The region of high negative voltages recorded with the CHARM-2 wafer corresponds to region of significant yield loss on the product wafers.

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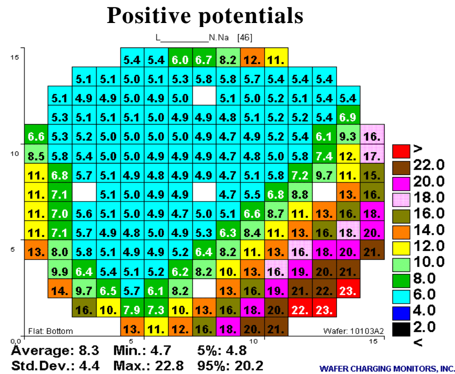
Wafer charging during Arsenic implants:

Bare wafers (no resist)

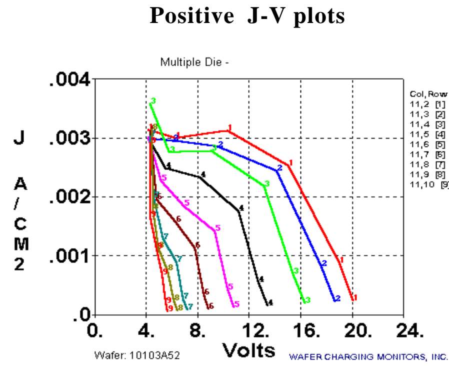
- **Arsenic; 4.5e15, 60 KeV, Ibeam = 19 mA, Flood = OFF**

  High positive potentials and current densities are recorded in lower right of the wafer.

Positive potentials



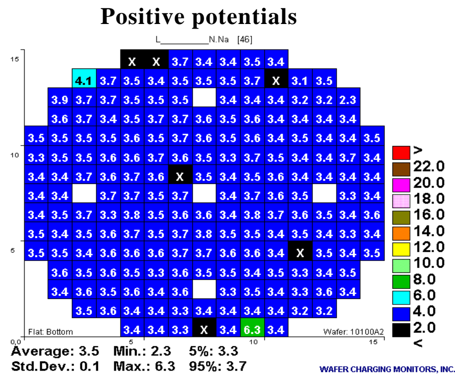
Positive J-V plots



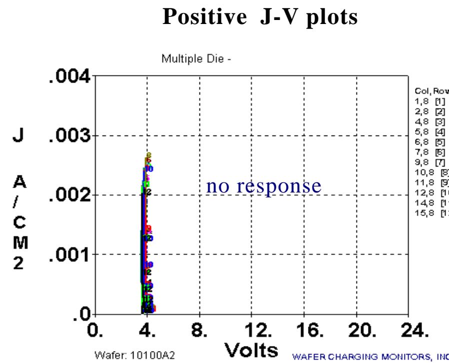
- **Arsenic; 4.5e15, 60 KeV, Ibeam = 19 mA, Flood = 6 A**

  Uniformly low positive potentials over the entire wafer. No charging currents detected.

Positive potentials



Positive J-V plots



The example at the top of the page shows that high positive potentials are recorded in the lower right of the wafer when the plasma flood system is turned OFF during a high-current Arsenic implant. The J-V graph shows the J-V plots recorded in individual die in column 11. The "1" J-V plot corresponds to die location (x=11, y=2), a region of high positive voltage and very high current density, while the "9" J-V plot corresponds to die location (x=11, y=10), a region of significantly reduced positive charging.

The example at the bottom of the page shows what happens when the plasma flood system is turned ON. The positive potentials are uniformly reduced all over the wafer, and no J-V plots are measured above 4 Volts.

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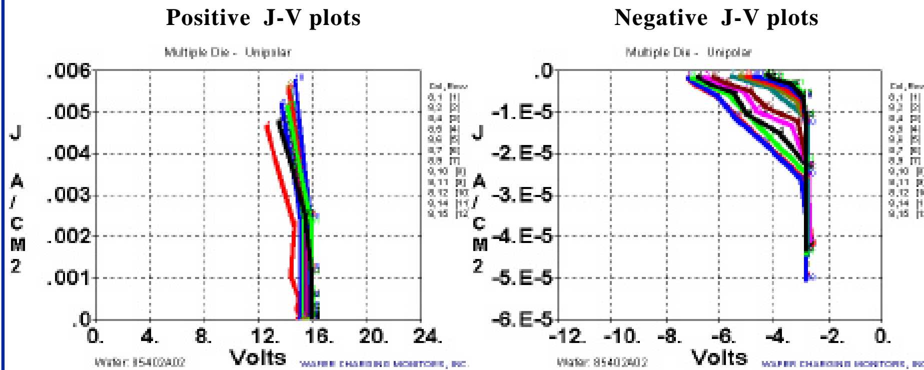
Electron flood effects during Arsenic implants:

Bare wafers (no resist)

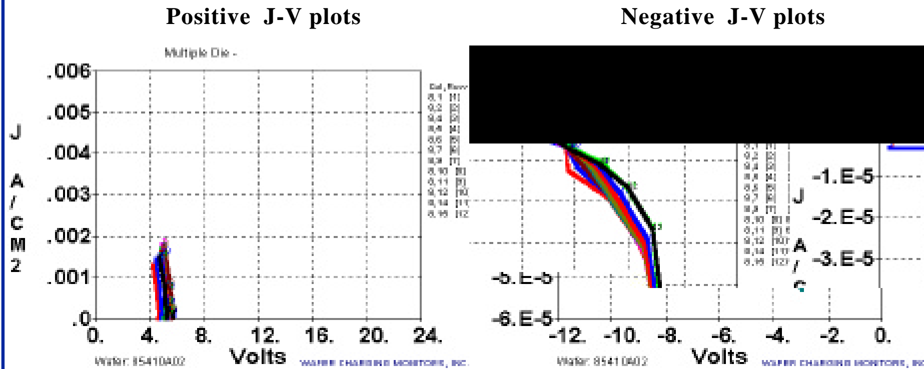
- **Arsenic; 5e15, 90 KeV, Ibeam = 20 mA, Flood = OFF**

Flood OFF: Positive J-V shifted to high voltages; negative J-V shifted to low voltages



- **Arsenic; 5e15, 90 KeV, Ibeam = 20 mA, Flood = ON**

Flood ON: Positive J-V shifted to low voltages; negative J-V shifted to high voltages



Here we illustrate the trade-off made between positive and negative charging during high-current Arsenic implants. The example at the top of the page shows positive J-V plots reaching high potentials when a device is under the beam while the electron flood system is turned OFF. This situation would result in severe damage, since positive charging is associated with high current densities.

To avoid this, the electron plasma flood system must be turned ON. As shown at the bottom of the page, this moves the positive J-V plots to low voltages where they will not cause damage. However, turning the electron flood system ON results in negative J-V plots which reach high negative potentials outside the beam. Now the high negative potentials may cause negative charging damage (since the long "tail" of the negative J-V plots is likely to intersect the gate oxide Fowler-Nordheim plot and force negative current into the gate oxide).

Since n-channel devices are particularly sensitive to negative charging, the trade-off between positive and negative charging must be made properly.

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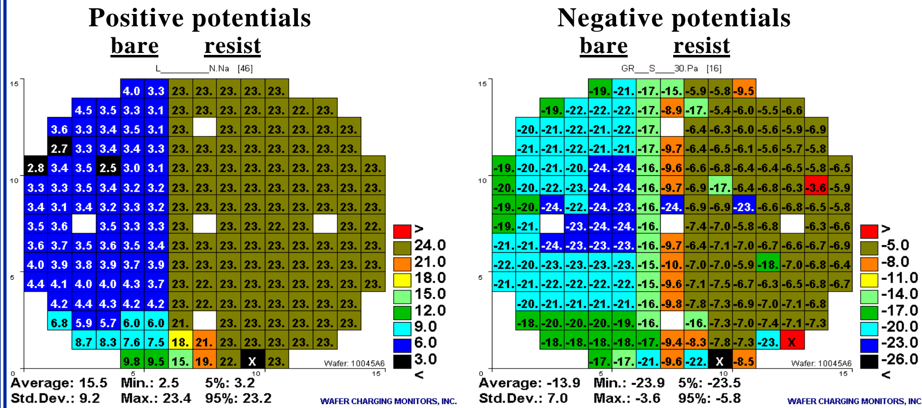
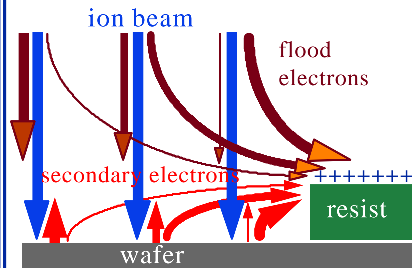
Resist effects during Arsenic implants:

Right half of wafer covered with resist, left half bare

- **Arsenic; 4e15, 80 KeV, I_{beam} = 3.8 mA, I_{disc} = - 4 mA**



- **Model for photoresist-enhanced wafer charging**



The positively charged resist attracts both the flood electrons and the secondary electrons generated by the high energy ion beam. This results in highest positive current densities nearest the resist edge. (Note that presence of resist shifts potentials toward more positive values.)

Ref.: W. Lukaszek, S. Reno, and R. Bammi, "Influence of Photoresist on Wafer Charging During High Current Arsenic Implant", Proceedings of Eleventh International Conference on Ion Implantation Technology, Austin, TX, June 16-21, 1996.

This is a simple example illustrating the significant influence that resist has on wafer charging during high-current ion implants. In this experiment, the right half of the wafer was covered with resist, while the left half was not covered with resist. Wafer maps of positive and negative potentials show that resist increases peak positive potentials and reduces peak negative potentials. Inspection of positive J-V plots horizontally across the wafer showed that the highest positive current densities were recorded nearest the resist edge, on the bare side of the wafer. This led us to propose the charging model shown at the bottom of the page.

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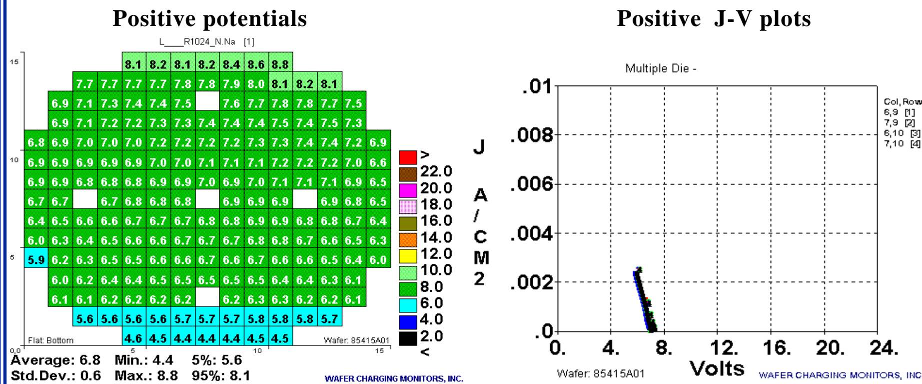
Resist effects during Arsenic implants:

Bare wafer vs. patterned-resist covered wafer

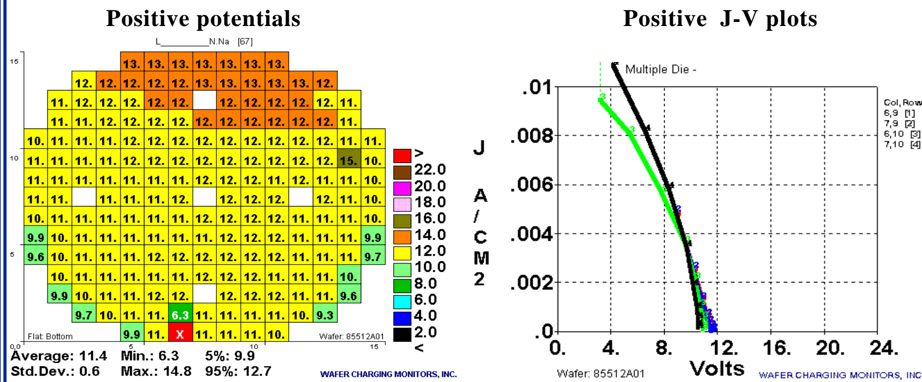
- **Arsenic; 2e15, 40 KeV, Jbeam = 1.1 mA/cm^2, Flood = ON**
  Bare wafer: **Low positive potentials; positive J-V plots occur at low voltages.**

Positive potentials **Positive J-V plots**



- **Arsenic; 2e15, 40 KeV, Jbeam = 1.1 mA/cm^2, Flood = ON**
  Resist-covered wafer: **High positive potentials; positive J-V plots shifted to high voltages.**

Positive potentials **Positive J-V plots**



This is another example of the influence of photoresist on wafer charging during high-current ion implants. Here, the comparison is between results obtained with a bare wafer and a wafer covered with resist patterned with a four-field mask designed to imitate the device/resist combinations which occur on products implanted with a dark-field mask (i. e. the implant is done through "holes" in the resist, while most of the wafer is covered with resist). Again, it is observed that the presence of resist shifts the positive J-V plots to higher voltages, where they may intersect the gate oxide Fowler-Nordheim plots and cause significant damage.

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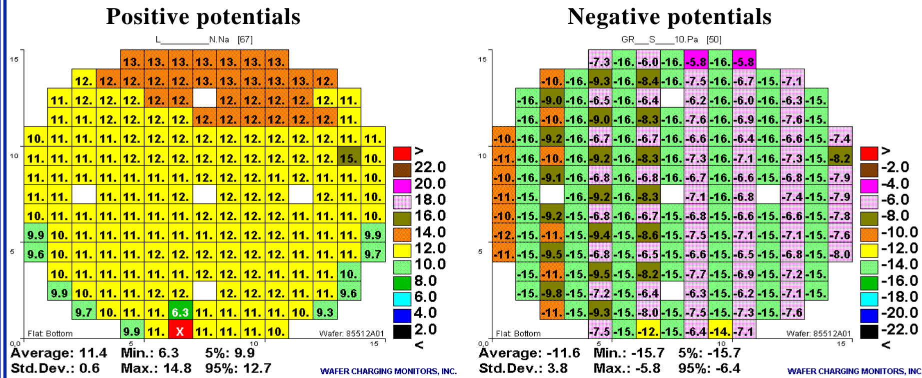
Patterned-resist effects during Arsenic implants:

Mask: four dark-fields, emulating resist placement on product wafers

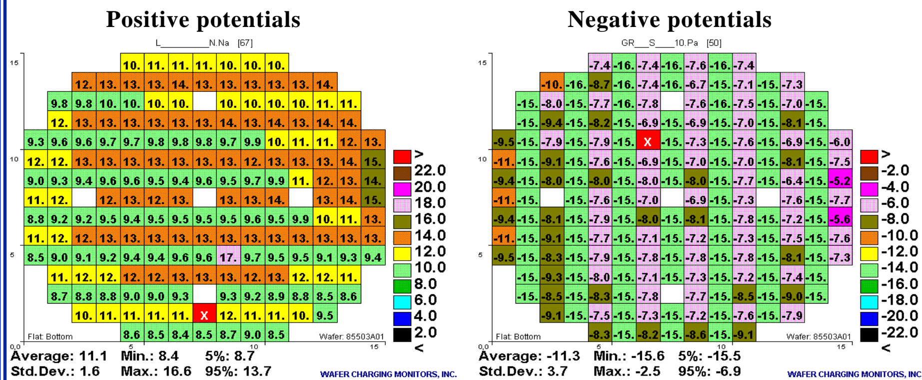
- **Arsenic; 2e15, 40 KeV, Jbeam = 1.1 mA/cm^2, Flood = ON**

Positive potentials do not depend on resist layout. Negative potentials depend on resist layout.



- **Arsenic; 2e15, 120 KeV, Jbeam = 1.2 mA/cm^2, Flood = ON**

Positive and negative potentials show different dependence on resist layout.



In this example, CHARM-2 wafers patterned with the same four-field dark-field mask were implanted at energies of 40 KeV (top) and 120 KeV (bottom). Significant differences in positive potentials are observed between different resist layouts at 120 KeV. Highest positive potentials and curent densities occur in cases where the gate is mostly covered with resist and only a small portion is exposed to the implant. In the case of the 40 KeV implants, no differences in positive potentials or current densities are observed with different resist layouts. However, at both 40 KeV and 120 KeV the negative potentials show another variation with resist layout - the highest potentials are observed when the gate, whether implanted or covered with resist, is disconnected from the resist on the field. These results were presented at the XII International Conference on Ion Implantation Technology (IIT'98). The IIT'98 papers describing these results in more detail are available from WCM.

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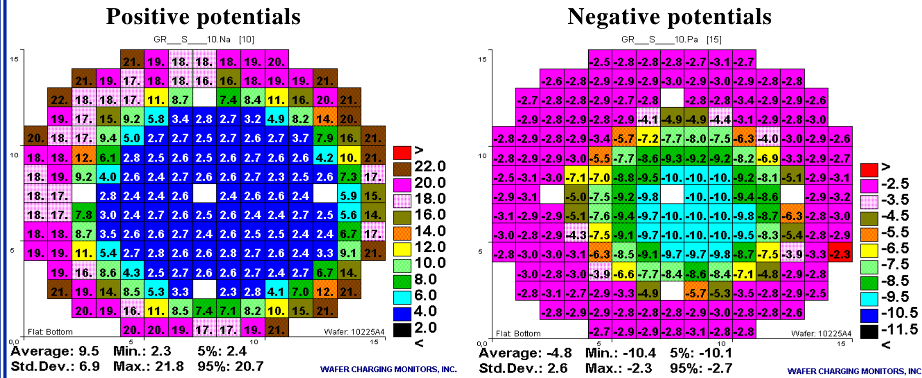
Wafer charging damage during resist ashing:

High current densities, NOT high potentials, are the cause of damage!

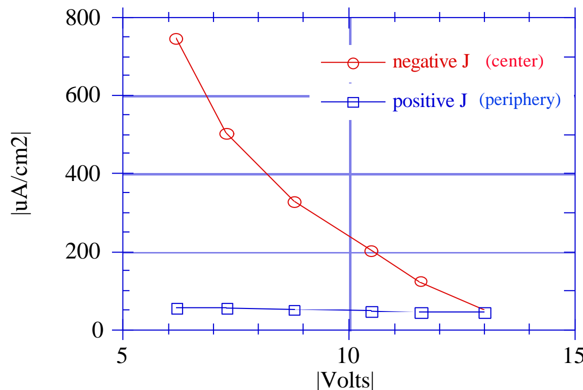
- **Positive and negative potentials**

  High positive potentials around wafer periphery; moderate negative potentials in center.



- **Positive and negative J-V plots**

  Low positive current density around wafer periphery; high negative current density in center.



Damage to 70 A gate oxides (observed on antenna capacitors) occurred in the center of the wafer, where the charge flux is greatest, NOT around wafer periphery, where the potentials are highest.

This example illustrates that regions of high potentials are not necessarily the regions of damage, and that regions of lower potentials are not necessarily free of damage. The positive potentials wafer map shows high positive voltages around the periphery of the wafer, while the negative potentials wafer map shows lower negative voltages in the center of the wafer. However, damage to 70 A antenna capacitors was observed in the center of the wafer. This result can be understood when the positive and negative current densities are taken into account. As shown in the graph at the bottom of the page, the negative current density (measured on die in the center of the wafer) is significantly higher than the positive current density (measured on die around the periphery of the wafer) at voltages which would cause charge conduction in 70 A oxides. Consequently, greater damage will be done by the negative currents, in the center of the wafer.

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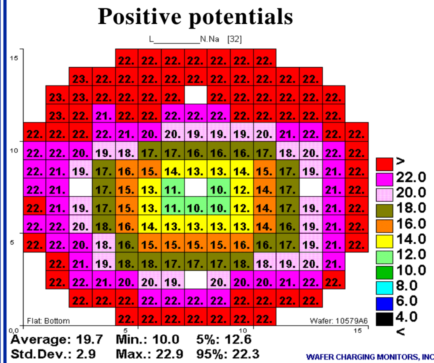
Wafer charging during polysilicon etching:

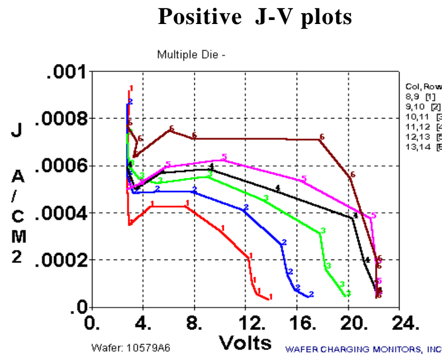
Start with high etch rate, but end with low etch rate to minimize damage.

• High etch rate process

High positive potentials and high positive current densities cause damage.

Positive potentials | **Positive J-V plots**

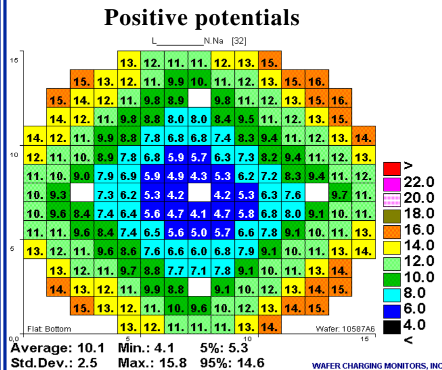


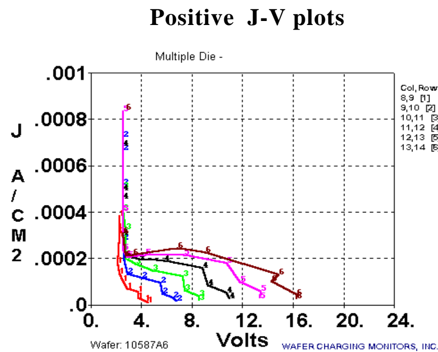


• Low etch rate process

Low positive potentials and low positive current densities cause no damage.

Positive potentials | **Positive J-V plots**





This is an example of process optimization to eliminate charging damage during polysilicon etching. As shown at the top of the page, the high-etch-rate process generates positive potentials which likely exceed 26 V around the periphery of the wafer (as determined from the shape of the positive J-V plots, which are saturated at 22 V). These high potentials are also accompanied by high positive current densities. On the other hand, the low-etch-rate process, shown at the bottom of the page, generates considerably lower potentials and lower current densities. (The four-fold symmetry of the positive potentials is due to four coils around the etching chamber, which are employed to generate the magnetic field used to increase plasma density.)

Since damage occurs after the polysilicon film is separated into individual "islands", the optimized process uses the high-etch-rate process to do most of the etching, followed by the low-etch-rate process to separate the polysilicon film into into individual "islands", and finish the etching. This procedure retains most of the high through-put of the high-etch-rate process, with the low damage of the low-etch-rate process.

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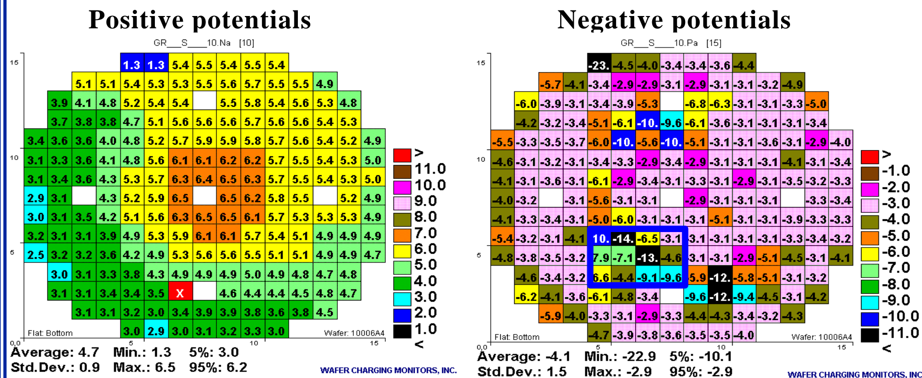
Wafer charging in ECR metal etcher:

Positive charging varies gradually, negative charging is very localized

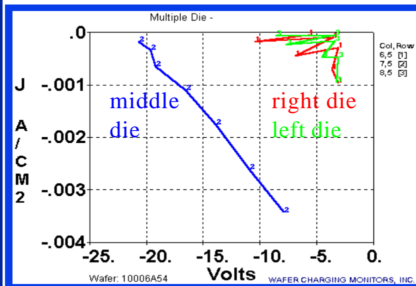
• High negative potentials are recorded in several spots

Positive potentials **Negative potentials**



• Intense negative charging confirmed with J-V plots

Negative J-V plots



Intense negative charging was recorded in the "middle" die (7,5). The die on the right and left side of die (7,5) recorded much lower current densities. The zig-zag pattern of the J-V plots recorded at these locations indicates rapid spatial variation in negative charging. The opposing zig-zag's confirm that most intense charging occurred in die (7,5). Similar behavior was observed at other locations on the wafer.

Ref.: W. Lukaszek, "Characterization of Wafer Charging in ECR Etching", 1997 2nd International Symposium on Plasma Process-Induced Damage, Monterey, CA, May 13-14, 1997.

Although the distribution of positive potentials is "well-behaved", the negative potentials wafer map indicates regions of highly localized negative charging. The negative J-V plots confirm this. Sigificant differences in negative potentials were observed on sensors less than 1 mm apart. This indicates that damage monitors used to analyze the charging characteristics of this tool must have high spatial resolution, and the ability to confirm the validity of isolated, anomalous results.

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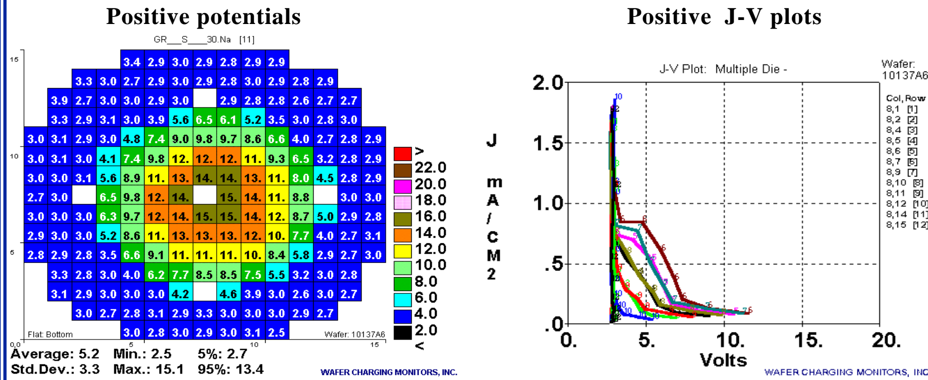
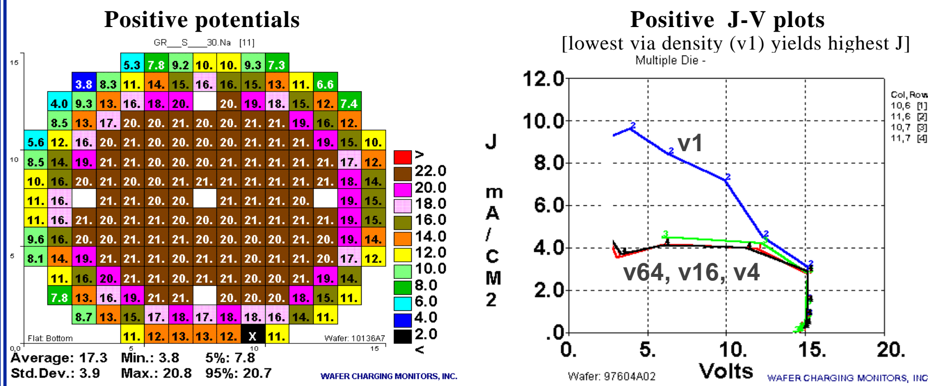
Patterned-resist effects during oxide etching:

Comparison of results obtained with bare and patterned-resist wafers

• Bare wafer shows moderate positive potentials and low current densities
(Positive charging is confined to a small area in the center of the wafer.)



• Resist-covered wafer shows high positive potentials and current densities
(Potential and current sensors are saturated at 21V. Positive curent sensors are saturated at 15V.



The presence of masked resist on the surface of the wafer can have a significant effect on the charging voltages and currents. The positive potentials and J-V plots measured with a bare CHARM-2 wafer during this oxide etch process are considerably lower than potentials and currents measured when a CHARM-2 wafer is covered with resist patterned with a four-field via mask. (Each field contains different density of vias: field v64 contains the highest density of vias, while field v1 contains the lowest density.) In this tool, the charging current also increases when the via density decreases.

It is also interesting to note that increased positive charging observed here is for 1.5um vias, where enhanced charging due to the "electron shading" effect should be negligible.

Reference: W. Lukaszek, J Shields, and A. Birrell, "Quantifying Via Charging Currents", 1997 2nd International Symposium on Plasma Process-Induced Damage, May 13-14, Monterey, CA.

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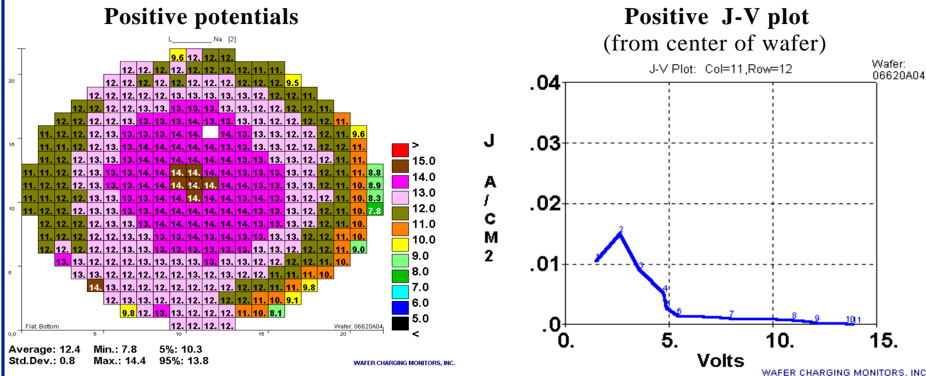
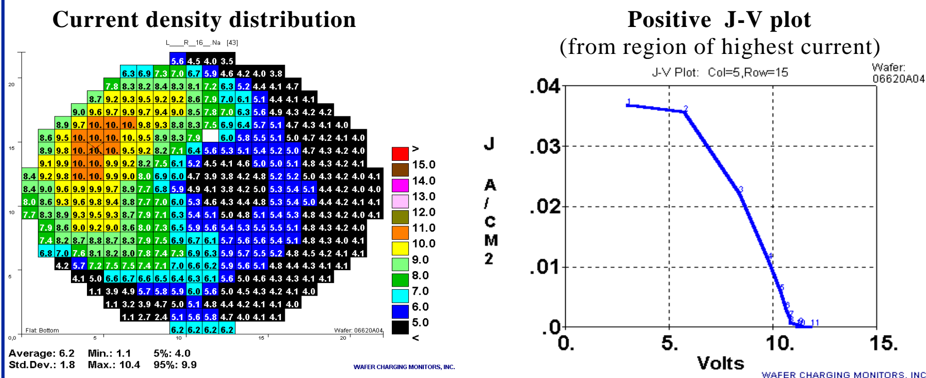
Wafer charging during oxide deposition:

Region of highest positive potentials is not the region of highest current

- **Highest positive potentials are recorded in the center of the wafer**
  (Lower J at low V implies charging occurred during different process step than was assumed.)



- **Highest current densities are recorded in the upper left of the wafer**
  (Charging damage will be greatest in upper left of the wafer, where current density is highest.)



Again, the region of highest positive potentials (center of the wafer; shown in the wafer map at the top of the page) is not the region of highest current density (upper-right portion of the wafer; shown in the wafer map at the bottom of page). In fact, the downward "dip" in the J-V plot from the center of the wafer implies that maximum positive potentials occurred for a very short time, and did not deliver maximum current density. The much higher positive current density in the upper-right portion of the wafer represents the steady-state.

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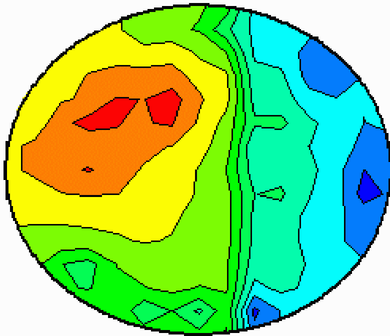
CHARM-2 used as equipment diagnostic:

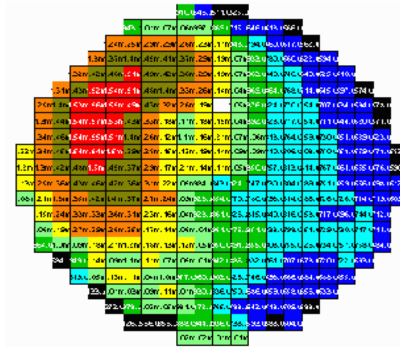
Distribution of current density coincides with ESC dielectric thickness

- **Comparison of contour plot of dielectric thickness of electrostatic chuck and CHARM-2 wafer map of positive current density**

Dielectric thickness of electrostatic chuck



CHARM-2 positive current density



- **User comment:**

… "The RF impedance is varying with the variation in dielectric thickness which results in high voltages and damage potential. I think this is a fine example of the diagnostic capabilities of your wafer. Without it, we would not have thought to measure it, and now specify, this hardware feature."

It was proposed that the non-uniform steady-state current distribution observed during the oxide deposition was due to non-uniform RF impedance of the electrostatic chuck. This appears to be the case, since the spatial variation in the thickness of the dielectric on the electrostatic chuck matches the distribution of the steady-state current density measured with the CHARM-2 wafer.

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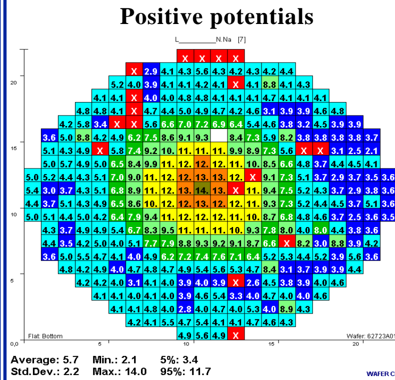
Wafer charging in etcher and asher cluster tool:

Masked 200 mm wafers

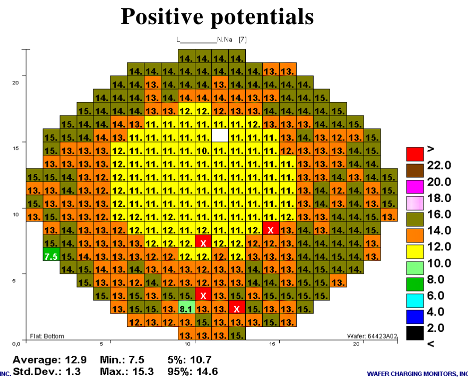
- **Positive charging in etcher**
  Highest positive potentials in center

Positive potentials



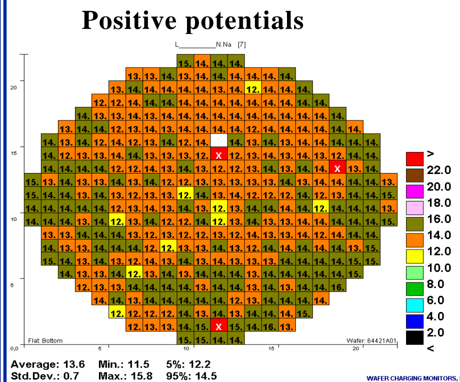
- **Positive charging in asher**
  Highest positive potentials around periphery

Positive potentials



- **Positive charging in etcher + asher**
  Uniformly high positive potentials

Positive potentials



The uniform positive charging observed on wafers after processing in the cluster tool resulted from the sum of positive charging in the etcher (highest positive charging in the center of the wafer) and the asher (highest positive charging around the periphery of the wafer).

To understand the origins of wafer charging damage on product wafers, it is important to use a monitoring tool such as CHARM-2 which can measure the charging environment of individual process tools (or individual chambers). In this example, the results obtained at the end of the unit process (etch + ash) show uniform positive charging over the entire wafer (bottom of page). However, this results from the superposition of the complementary charging by the etching process (which causes maximum positive charging in the center of the wafer), and the ashing process (which causes maximum positive charging around the periphery of the wafer).

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Application of CHARM-2 monitors:

- CHARM-2 monitors have been used for:

✓ new equipment selection
✓ equipment acceptance tests
✓ equipment calibration
✓ equipment benchmarking
✓ equipment problem diagnosis
✓ new equipment development
✓ identifying equipment responsible for yield loss
✓ process optimization
✓ maintenance scheduling
✓ studies of basic charging mechanisms
✓ studies of photoresist-mediated wafer charging
✓ UV lamp qualification