Quantifying Wafer Charging During Via Etch

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Abstract

A CHARM™-2 investigation of wafer charging during via etching shows that wafer surface conditions strongly influence the observed results. Under identical process conditions, bare wafers underestimate the charging results. When wafers are covered with patterned resist, much higher surface-substrate potentials and current densities are observed.

I. Introduction

This paper describes an investigation of wafer charging associated with a via etch process performed on six inch wafers in the LAM 384T triode etcher, prompted by equipment modifications and gate oxide failures at poly edge on product wafers observed during failure analysis. (Possible contribution by ion implant was ruled out through other experiments.) In order to minimize the confounding effects which can arise when dealing with complex product wafers and multi-step process flows, it was decided to use a product/process independent test vehicle, which could provide a direct measure of the various phenomena associated with charging effects in plasma-based process equipment. The CHARM™-2 wafers, populated with electrostatic potential, current density, and UV sensors, were chosen as the test vehicle [1]. Since charging problems often depend on multiple factors, it was decided to proceed in stages to minimize possible confusion. First, the charging properties of the equipment were established by exposing bare CHARM™-2 wafers to the via etch process. Next, CHARM™-2 wafers were coated with resist and exposed to the via etch process. Finally, CHARM™-2 wafers were coated with resist, patterned with the via mask, and exposed to the via etch process. As shown in the following, different results were obtained in each case, underscoring the importance of duplicating the surface conditions which exist on product wafers when employing test vehicles to evaluate equipment charging characteristics.

II. Description of CHARM-2

In order to make the following results more meaningful, it is important to understand the capabilities of the CHARM™-2 technique. The 150mm CHARM™-2 wafers contain 188 sites populated with EEPROM-based, calibrated, polarity-sensitive sensors of wafer surface-substrate potentials, net charge flux, and UV dose [1].

The CHARM™-2 potential sensors are implemented by connecting a charge collection electrode (CCE) on the surface of the wafer to the control-gate of an EEPROM transistor, as shown in **Figure 1**.   The CHARM™-2 potential sensors thus resemble the widely used "antenna" devices, employing gate oxide capacitors or transistors, except that in CHARM™-2 the sensing element is not gate oxide, but a EEPROM transistor, whose threshold voltage is changed by the voltage developed on the CCE.

In order to maximize the low-voltage sensitivity of the potential sensors, and to determine the polarity of the collected charge, the CHARM™-2 potential sensors make use of the full range of response of the CHARM™-2 EEPROM transistors.   This response is shown in **Figure 2**, as a plot of the Vg vs. Vt characteristics, obtained by sweeping the control-gate voltage between Vg = +30V and Vg = - 30V, and measuring the threshold voltage at each value of control-gate voltage.   From **Figure 2,** it becomes apparent that a CHARM™-2 EEPROM transistor programmed to a "saturated *positive*" threshold state responds linearly to *negative* Vg, while CHARM™-2   EEPROM transistor programmed to a "saturated *negative*" threshold state, responds linearly to *positive* Vg. Consequently, two sensors are used to determine the polarity and magnitude of the potential developed by charge collected on a CCE. One sensor, whose EEPROM is programmed to a saturated *positive* threshold state, is used to measure the magnitude of *negative* potential by determining the value of Vg which corresponds to the value of Vt measured on the EEPROM transistor *after* exposure of the CHARM™-2 wafer to a charging environment. (For example, a post-experiment Vt = 5V implies that a surface-substrate potential Vg = -12V was developed on the CHARM™-2 wafer as result of exposure to the charging environment.)   Conversely, another sensor whose EEPROM is programmed to a saturated *negative* threshold state is used in an analogous manner to measure the magnitude of *positive* surface-substrate potential.

The CHARM™-2 charge-flux sensors are implemented by adding current-sensing resistors between the CCE and the substrate of the potential sensors, as shown **Figure 3**. In this configuration, the EEPROM transistor is used to measure the voltage across the current-sensing resistor, from which the current density may be determined. The charge-flux sensors are also implemented in pairs, where one sensor is used to measure negative charge flux and the second sensor is used to measure positive charge flux.

Since charge flux experienced by wafers in IC process equipment can vary over a large range, CHARM™-2 wafers implement many pairs of charge-flux sensors to span a range of four and a half orders of magnitude in current densities. The closely ratioed current-sensing resistors permit reconstruction of the J-V characteristics of the charging source from the charge-flux sensor data, as shown in **Figure 4**. (In the J-V plane, each resistor is represented by a straight line with a slope of 1/R. Since the response of each sensor must lie on that line, each sensor provides one point in the J-V plane, and the collection of (J,V) values obtained from the set of CHARM™-2 current sensors allows re-construction of the J-V characteristics of the charging source.) The set of CHARM™-2 charge-flux sensors thus implements a passive plasma probe (analogous to a Langmuir probe) capable of quantifying, on the wafer surface, that portion of the plasma J-V characteristic where the plasma delivers power to the wafer, which is responsible for device damage.

III. Experimental results

In the first experiment, bare CHARM™-2 wafers were exposed to the via etch process. Moderately high positive surface-substrate potentials (13V-15V) were recorded in the center of the wafer, as shown in **Figure 5,** indicating a plasma non-uniformity **[2].** Corresponding positive J-V plots for the die marked "X" are shown in **Figure 6.** Negative potential and charge flux sensors did not respond, indicating that negative potentials did not exceed -3.5V. Slightly higher UV dose was recorded in the center of the wafer.

In the second experiment, the CHARM™-2 wafers were coated with photoresist and exposed to the via etch. This time, very high positive potentials (in excess of 20.5V, sensors saturated) were recorded over a much larger portion of the wafer, as shown in **Figure 7,** while current sensors did not respond, indicating that positive charge flux did not exceed 10uA/cm². Negative potentials reached -11.5V in the center of the wafer, in a pattern resembling **Figure 5.** Negative current sensors did not respond, indicating that charge flux did not exceed -10uA/cm². The observation that charge flux sensors did not respond is not surprising, since the wafer was coated

with resist, an insulator. However, the greatly elevated positive potentials observed on the CCEs (under the resist) indicate that positive potentials in excess of several tens of volts must have existed on top of the resist.

The highly elevated potentials on top of the resist suggested the troubling possibility that in the presence of holes in the resist, as would exist during a via etch, high positive potentials *and* high curent densities might exist - a condition which could lead to device damage. Consequently, a third experiment was performed using a CHARM™-2 wafer covered with resist patterned with the product via mask. As shown in **Figure 8,** the region of saturated positive potentials (> 22V) is slightly smaller. The response of the charge flux sensors is highly irregular, since the product via mask does not align to the CHARM™-2 layout, resulting in random exposure of the CCEs to the charge flux, except at the scribe lanes, as shown for one charge flux sensor in **Figure 9.** (Different patterns of this kind are observed for different sensors due to differences in sensor location.) Positive J-V plots corresponding to the die locations marked "X" are shown in **Figure 10.** Although the J-V plots are very irregular, due to the lack of alignment of the charge flux sensor CCEs to the via mask, resulting in varying amount of exposed CCE area to the charge flux, it is clear that *both* high current densities (note change of J scale) *and* high positive potentials (likely exceeding the breakdown voltage of the 25nm gate oxide) now exist. The charge flux sensors saturated at ~22V, so it is not possible to determine the voltage at which J → 0. However, J ≥ (2.3)1.4mA/cm² was recorded at ~22V, and J ≥ (2.3)3.6mA/cm² was recorded at ~16V, whereas at the same voltages J < 10uA/cm² on bare wafers. (The multiplicative factor of 2.3 takes into account the difference in CCE area used in the software which generated the J-V plots in Figure 10, vs. the actual CCE area exposed by the scribe lane.) Consequently, during overetch the plasma will be able to supply current to gate oxides of transistors whose gates are connected to the exposed metalization, and may cause device damage.
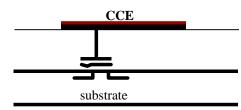
IV. Conclusions

The CHARM™-2 results reported here show that the presence of resist on the surface of the wafer greatly enhances the potentials and charge fluxes experienced by the wafers during via etch. Investigations of charging phenomena associated with contact or via etch should take this into account, as well as the layout features of the photoresist mask. This investigation is still in progress. Additional experiments using via masks customized to the CHARM™-2 layout will be performed to better understand the influence of photoresist layout parameters affecting these phenomena.

Similar experiments are planned for other etch steps to determine their relative contribution to the observed oxide failure results.
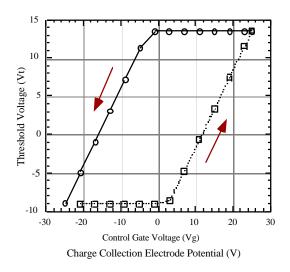
V. References

[1] W. Lukaszek, "The Fundamentals of CHARM™-2", Technical Note 1, Wafer Charging Monitors, Inc., 127 Marine Road, Woodside, CA, 94062.
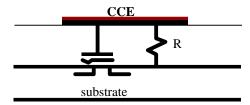[2] S. Fang, S. Murakawa, and J. McVittie, "Modeling of Oxide Breakdown from Gate Charging During Resist Ashing", IEEE Trans. El. Dev., Vol. 41, No. 10, October 1994, pp. 1848-1855.
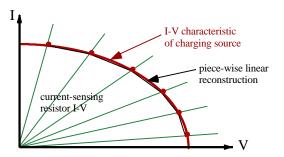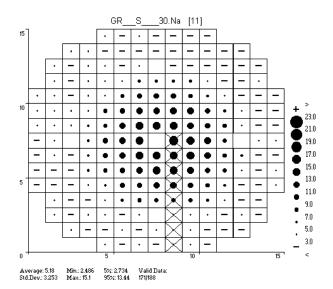
Figure 1. CHARM™-2 potential sensor.

Figure 2. Vg vs. Vt characteristics of CHARM™-2 EEPROM transistor.

Figure 3. CHARM™-2 charge-flux sensor.

Figure 4. Charge-flux sensors with different value current sensing resistors allow re-construction of the J-V characteristics of the charging source, implementing a passive plasma probe.

Figure 5. Positive potentials on bare wafer; "X" indicates die location selected for J-V plot in Figure 6.
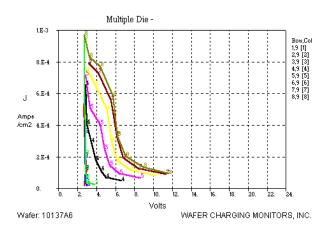

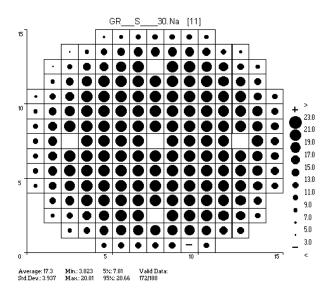**Figure 6.** Positive J-V plots obtained on bare wafer.

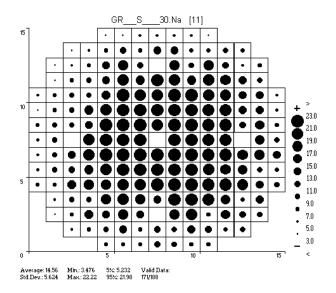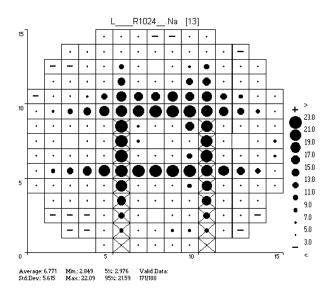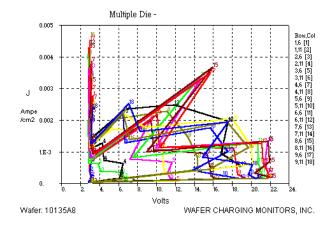**Figure 7.** Positive potentials on resist-covered wafer.

Figure 8. Positive potentials on wafer covered with resist patterned with product via mask.

Figure 9. Positive potentials across current sensor on wafer covered with resist patterned with product via mask; "X" indicates die location selected for J-V plot in Figure 10.

Figure 10. Positive J-V plots obtained on on wafer covered with resist patterned with product via mask. J-V plots are irregular due to mis-alignment of via mask and CHARM™-2 wafer layout. (Note change in J scale. To obtain actual J values, the above results must be multiplied by at least 2.3)